A Practical Method to Model Effective Permittivity and Phase Delay Due to Conductor Surface Roughness

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Speaker

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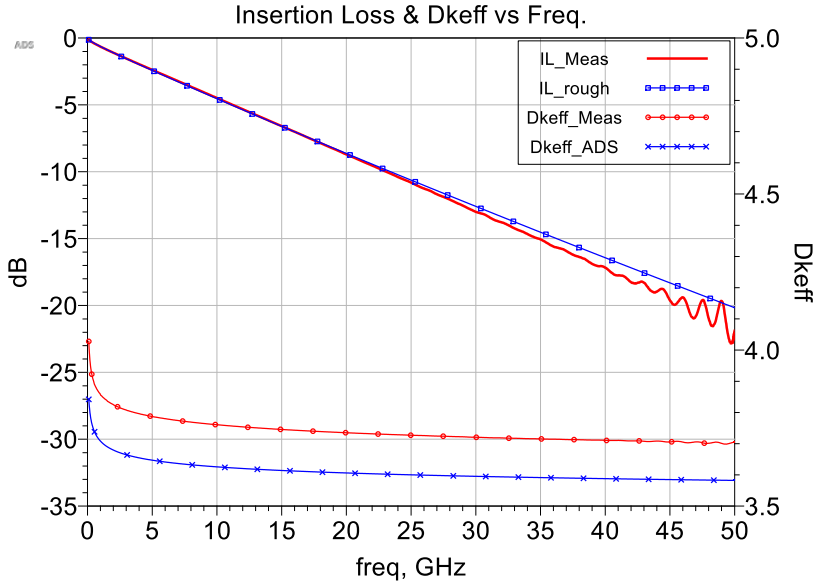
Lambert (Bert) Simonovich graduated in 1976 from Mohawk College of Applied Arts and Technology, Hamilton, Ontario Canada, as an Electronic Engineering Technologist. Over a 32-year career, working at Bell Northern Research/Nortel, in Ottawa, Canada, he helped pioneer several advanced technology solutions into products. He has held a variety of engineering, research and development positions, eventually specializing in high-speed signal integrity and backplane architectures. After leaving Nortel in 2009, he founded Lamsim Enterprises Inc., where he continues to provide innovative signal integrity and backplane solutions as a consultant. He has also authored and coauthored several publications, which are posted on his web site at www.lamsimenterprises.com. His current research interests include: high-speed signal integrity, modeling and characterization of high-speed serial link architectures.

Acknowledgements

- Dr. Alexandre Guterman
- Dr. Eric Bogatin

Modeling Issue

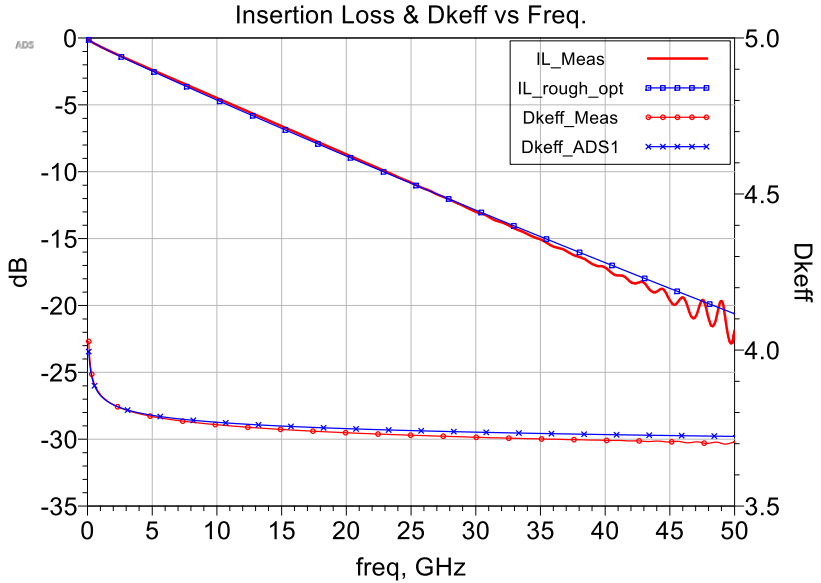


Modeling transmission lines from data sheet parameters:

$\Rightarrow$ Discrepancy in D_{keff}

$\Rightarrow$ Inaccuracy in simulated IL

Modeling Issue



Accuracy of IL greatly improved when measured D_{keff} is used:

Study by Al Horne et al [3]

0.5μm RMS

0.7μm RMS

1.5μm RMS

3.0μm RMS

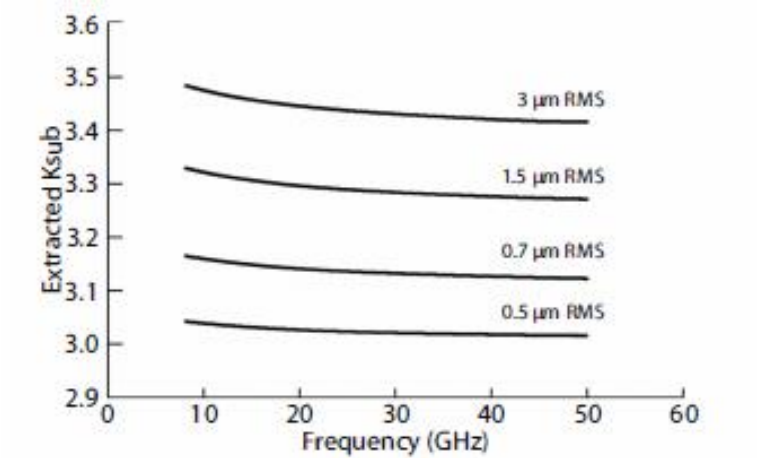
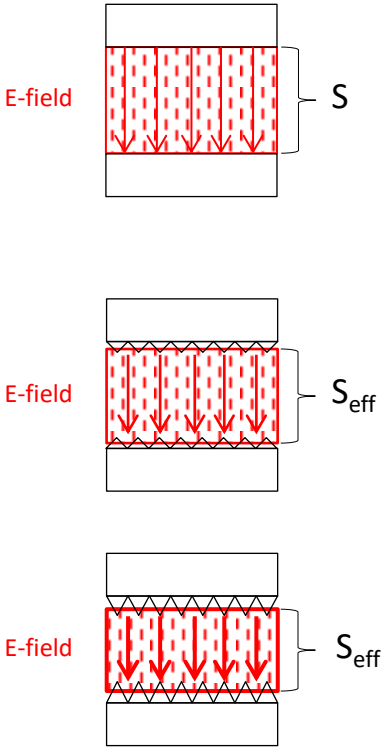


Chart reference [3]

The rougher copper profile the higher D_{keff} for the same dielectric thickness

Theory



As roughness profile increases:

- Effective separation decreases
- E-field strength increases
- Capacitance increases
- D_{keff} increases
- Phase Delay increases

Motivation

Develop a method to accurately predict D_{keff} and phase delay due to conductor surface roughness profile, as published in manufacturers' data sheets, without relying on measured data for curve fitting

Outline

- Background
- Gauss' Law
- Parallel Plate Capacitor
- Conductor Roughness
- Modeling D_{keff} Due to Roughness
- Validating the Model
- Case Studies

Permittivity

Ability of a dielectric material to store electrical energy in an electric field

In PCB industry:

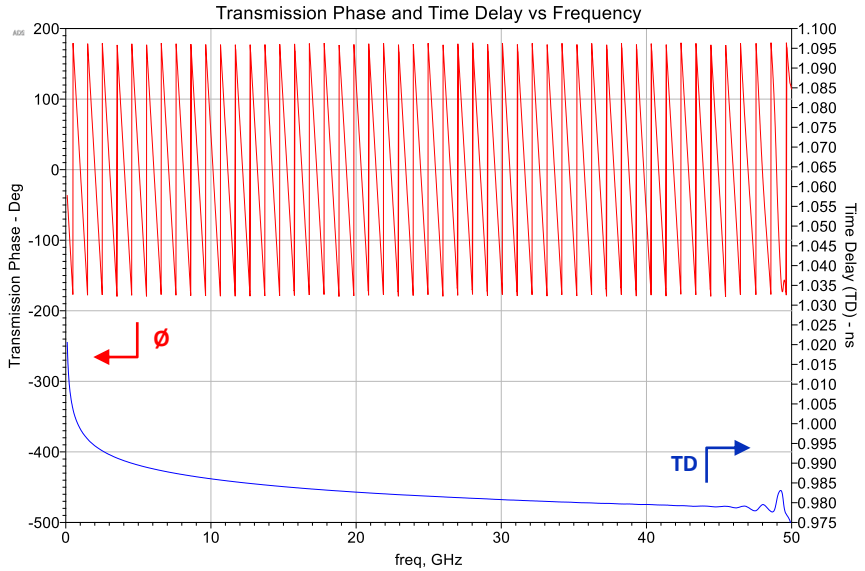
- Relative permittivity (ε_r) <=> Dielectric Constant (D_k)
- Effective permittivity (ε_{reff}) <=> D_{keff}

Effective D_k

Wadell [6] defines D_{keff} as the ratio of the actual structure`s capacitance to the capacitance when the dielectric is replaced by air.

$$D_{keff} = \frac{C_{actual}}{C_{air}}$$

Phase Delay



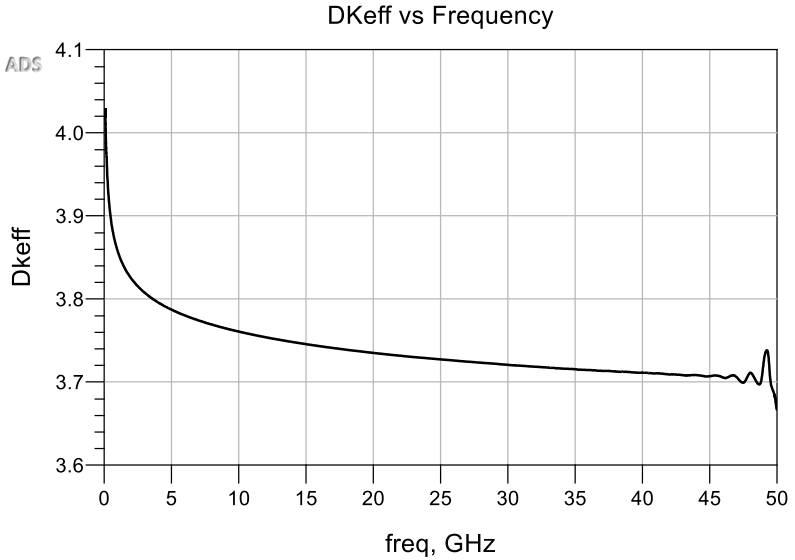
Phase delay a.k.a. time delay (TD) in seconds can be derived from the transmission phase angle [2]*

$$TD(f) = -1\left[\frac{unwrap\left(phase\left(S21\right)\right)}{360 \times freq}\right]$$

Simulated with Keysight ADS [15]

* Keysight ADS [15] equation syntax.

Effective Dielectric Constant (D_{keff})



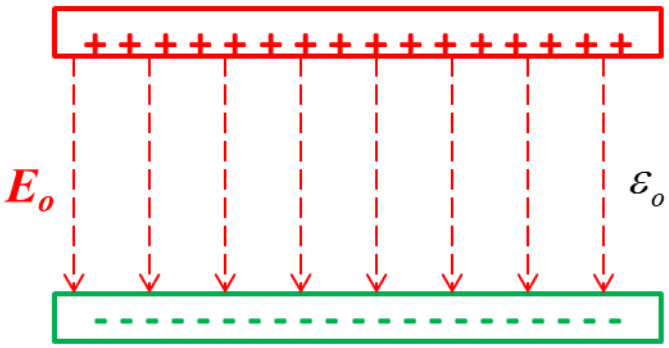
TD can be used to determine D_{keff}

$$D_{keff}(f) = \left(TD(f) \frac{c}{Length} \right)^2$$

Simulated with Keysight ADS [15]

Application of Gauss's Law

Gauss's Law

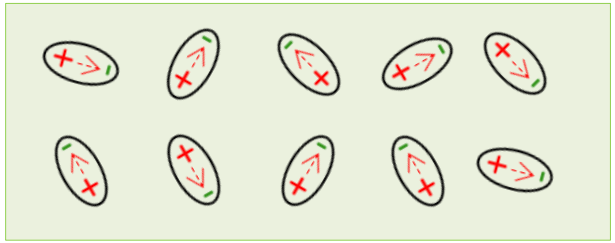


$$E_0 = \frac{\text{Surface Charge Density}}{\text{Permittivity Free Space}} = \frac{\sigma}{\varepsilon_0}$$

Relates the distribution of electric charge to resulting e-field

Can be used to determine the e-field between two oppositely charged parallel plates

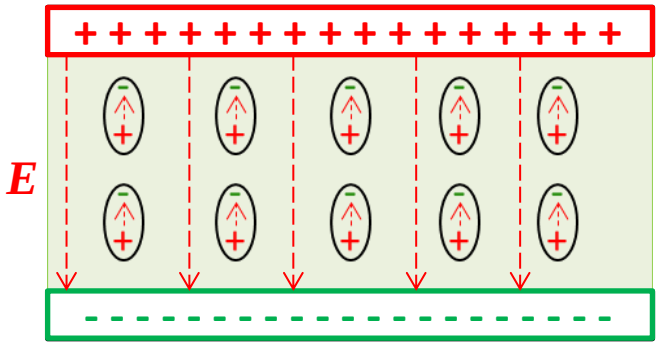
Dipoles in Dielectric Material in the Absence of E-field



Dielectric materials are insulators often composed of polar molecules

Look electrically like small dipoles that line up randomly

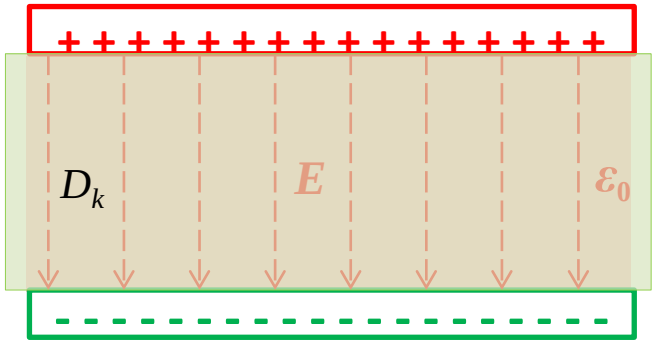
Polarization of Dipoles in Presence of E-field



E-field of the dipoles (E_D) opposes e-field in free space (E_0) to yield a net e-field intensity (E)

$$E = E_0 - E_D$$

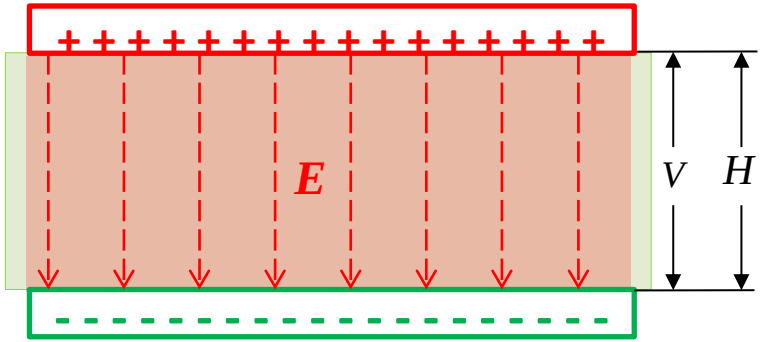
E-field Intensity in Presence of Dielectric



Insertion of dielectric material reduces the e-field intensity inversely proportional to D_k

$$E = \frac{\sigma}{D_k \varepsilon_0}$$

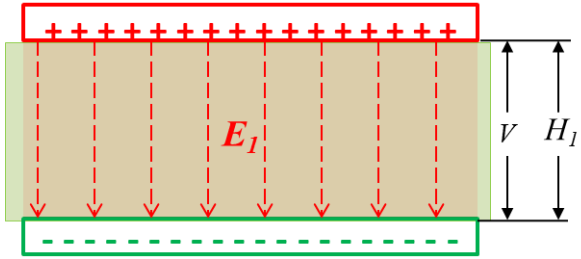
E-field vs Parallel Plate Separation



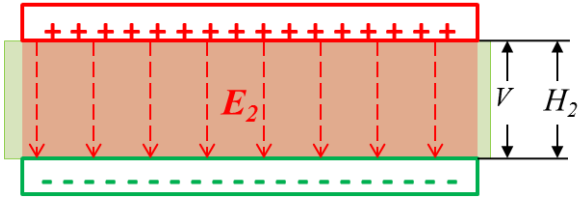
Electric field intensity can also be expressed as the ratio of volts to distance between two plates

$$E = \frac{V}{H}$$

E-field Intensity vs Parallel Plate Separation



$$E_1 = \frac{V}{H_1}$$

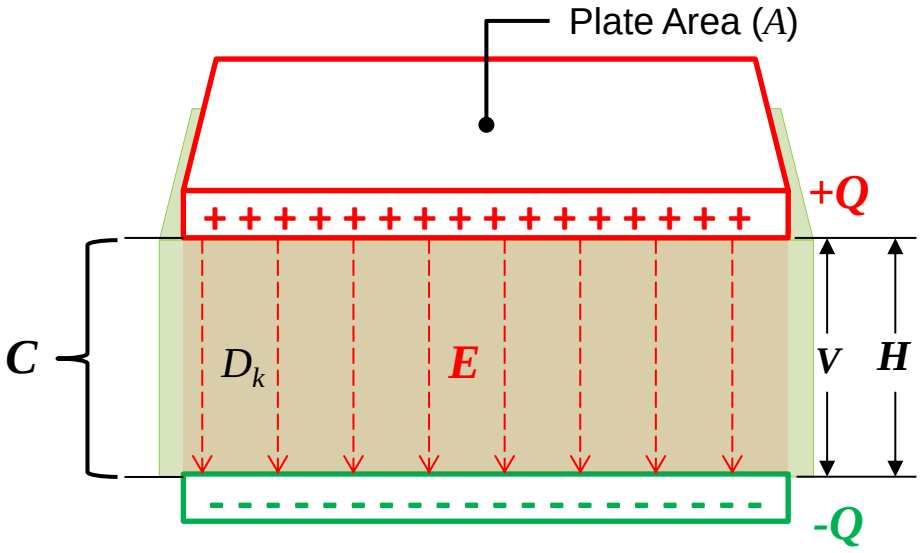


$$E_2 = \frac{V}{H_2}$$

$$\therefore \quad \frac{E_2}{E_1} = \frac{H_1}{H_2}$$

Parallel Plate Capacitor

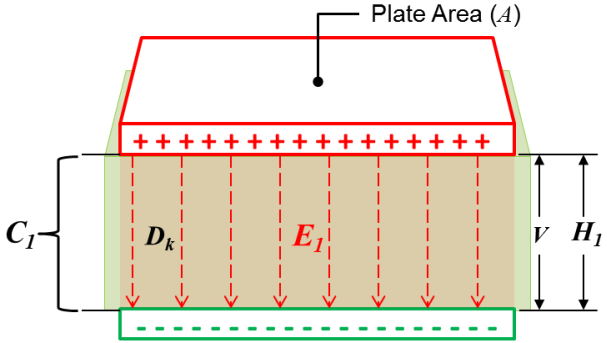
Parallel Plate Capacitor



Any structure capable of storing an electric charge is called a capacitor

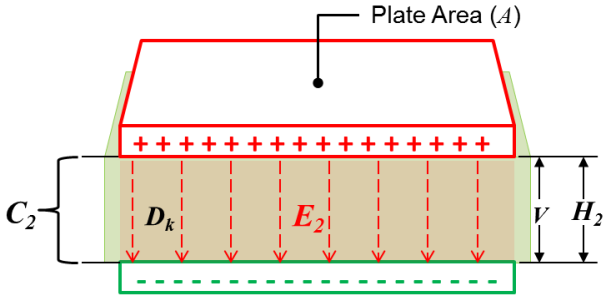
$$C = \frac{Q}{V} = \frac{D_k \varepsilon_O A}{H}$$

E-field Intensity vs Parallel Plate Capacitor



$$C_1 = \frac{D_k \varepsilon_O A}{H_1}$$

$$E_1 = \frac{V}{H_1}$$



$$C_2 = \frac{D_k \varepsilon_O A}{H_2}$$

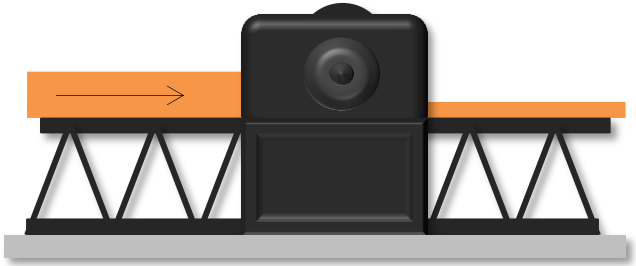
$$E_2 = \frac{V}{H_2}$$

$$\therefore \quad \frac{C_2}{C_1} = \frac{H_1}{H_2} = \frac{E_2}{E_1}$$

Conductor Roughness

Copper Foil Manufacturing Processes

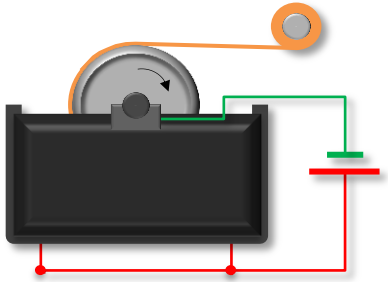
Rolled



Smoother

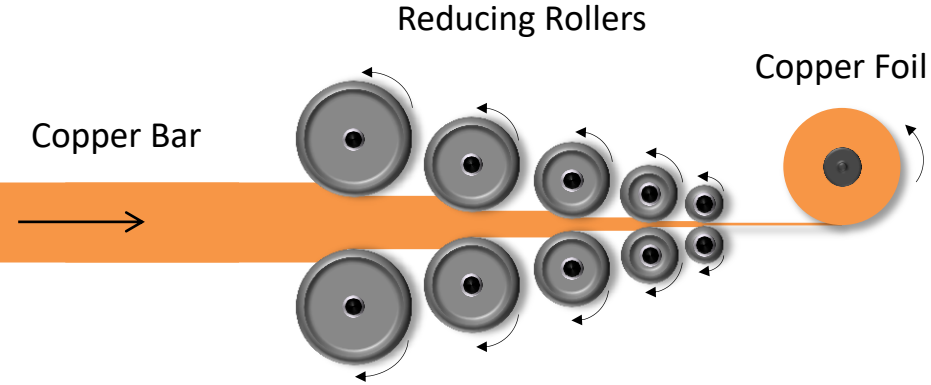
VS

Electro-deposited (ED)



Lower Cost

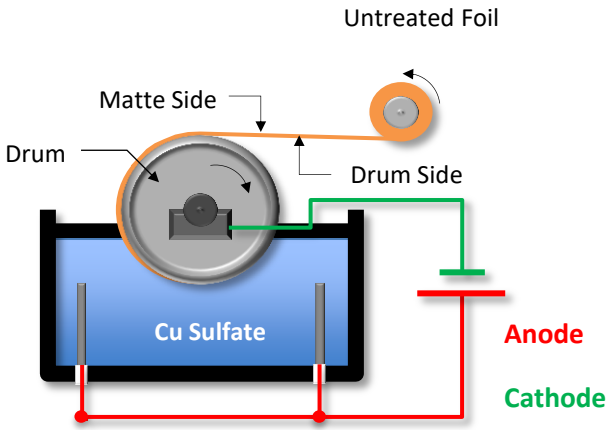
Rolled Copper Foil Fabrication Process



Copper bar fed through a series of progressively smaller rollers to achieve final thickness

Roller smoothness determines final smoothness of foil

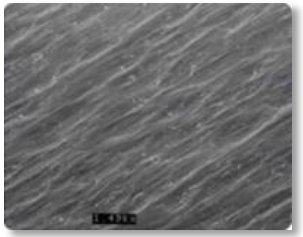
Electrodeposited Copper Foil Fabrication Process



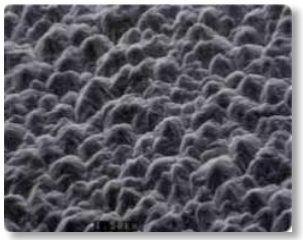
Drum speed controls foil thickness

Matte side always rougher than drum side

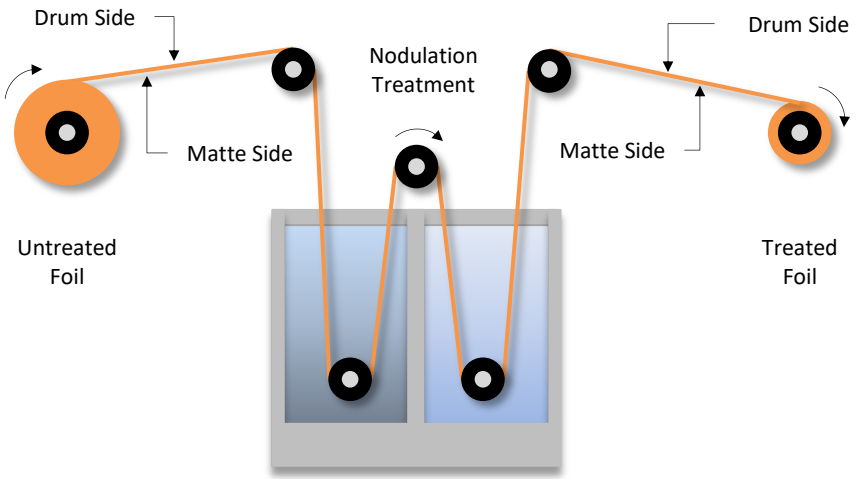
Electro-deposited Copper Foil Nodulation Treatment



Drum Side Untreated



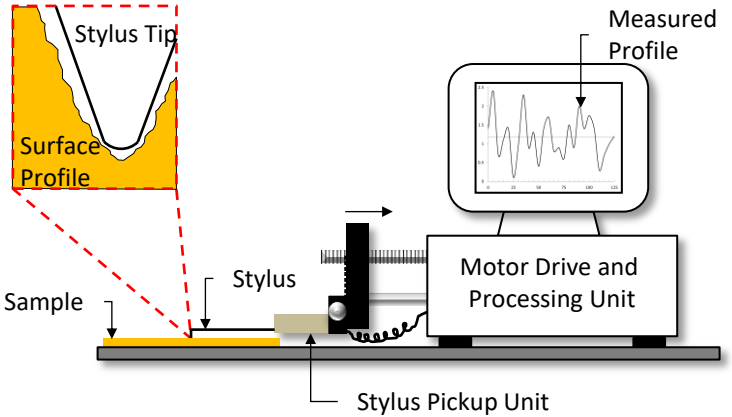
Matte Side Untreated



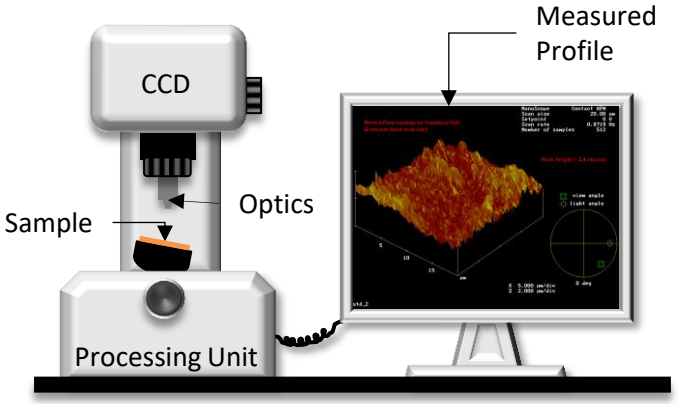
Drum Side Treated

Matte Side Treated

Profilometers Used to Measure Surface Roughness

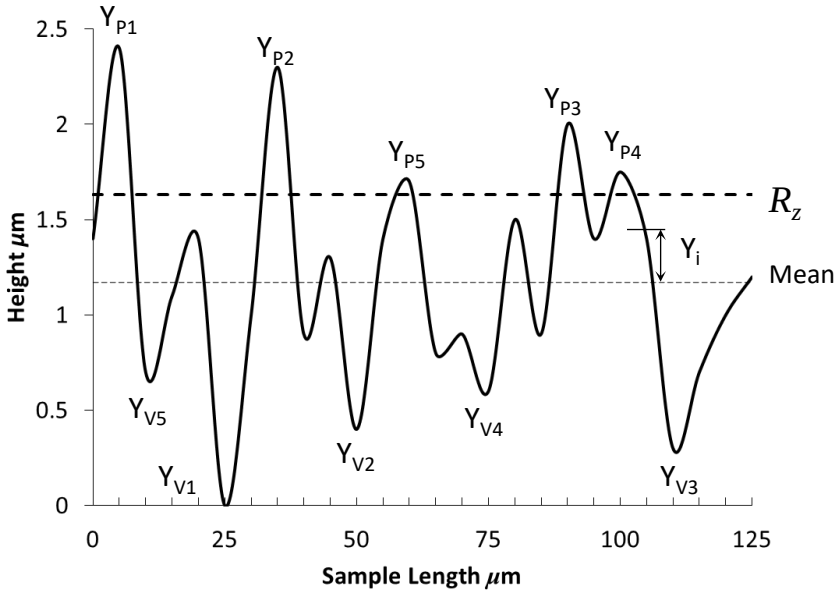


- ✓ Provides 2D Scan Profile
- ✓ Slow
- ✓ Less reliable
- ✓ Less accurate



- ✓ Provides 3D Scan Profile
- ✓ Faster
- ✓ More reliable
- ✓ More accurate

Roughness Parameters



Average (R_a)

$$R_a = \frac{1}{N}\sum_{i=1}^{N}|Y_i|$$

10-point Mean (R_z)

$$R_z = \frac{1}{5}\sum_{i=1}^{5}|Y_{Pi}| + \frac{1}{5}\sum_{i=1}^{5}|Y_{Vi}|$$

Modeling D_{keff} Due to Roughness

Rogers LCP Roughness Study [3]

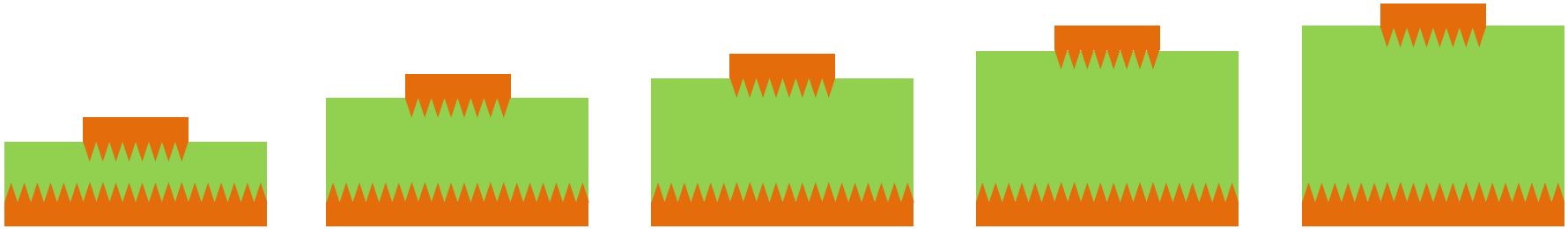
0.4μm RMS
t = 4 mils

0.4μm RMS
t = 8 mils

0.4μm RMS
t = 12 mils

0.4μm RMS
t = 16 mils

0.4μm RMS
t = 20 mils



3.0μm RMS
t = 4 mils

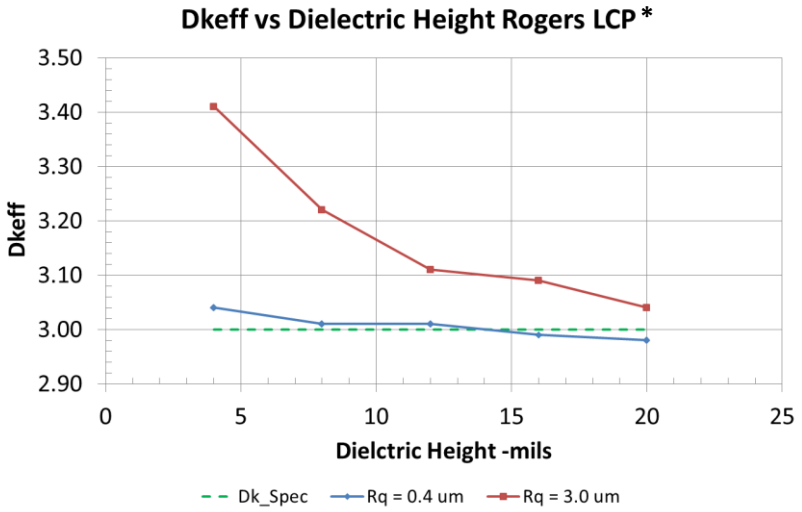
3.0μm RMS
t = 8 mils

3.0μm RMS
t = 12 mils

3.0μm RMS
t = 16 mils

3.0μm RMS
t = 20 mils

Rogers LCP Roughness Study [3]



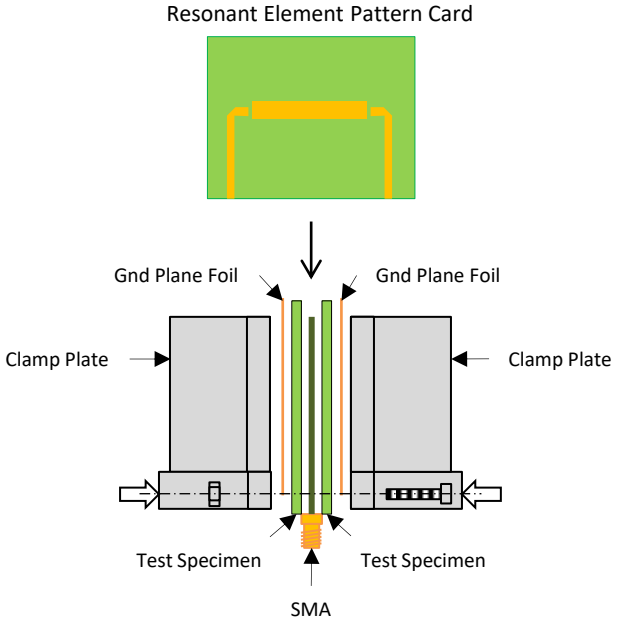
As thickness of the dielectric increased D_{keff} decreased

The rougher copper profile the higher D_{keff} for the same dielectric thickness

✓ Supports theory that higher roughness profile adds excess capacitance thereby increasing D_{keff} due to reduced separation between plates

* LCP = Liquid Crystal Polymer

Clamped Stripline Resonator Test Method [8]

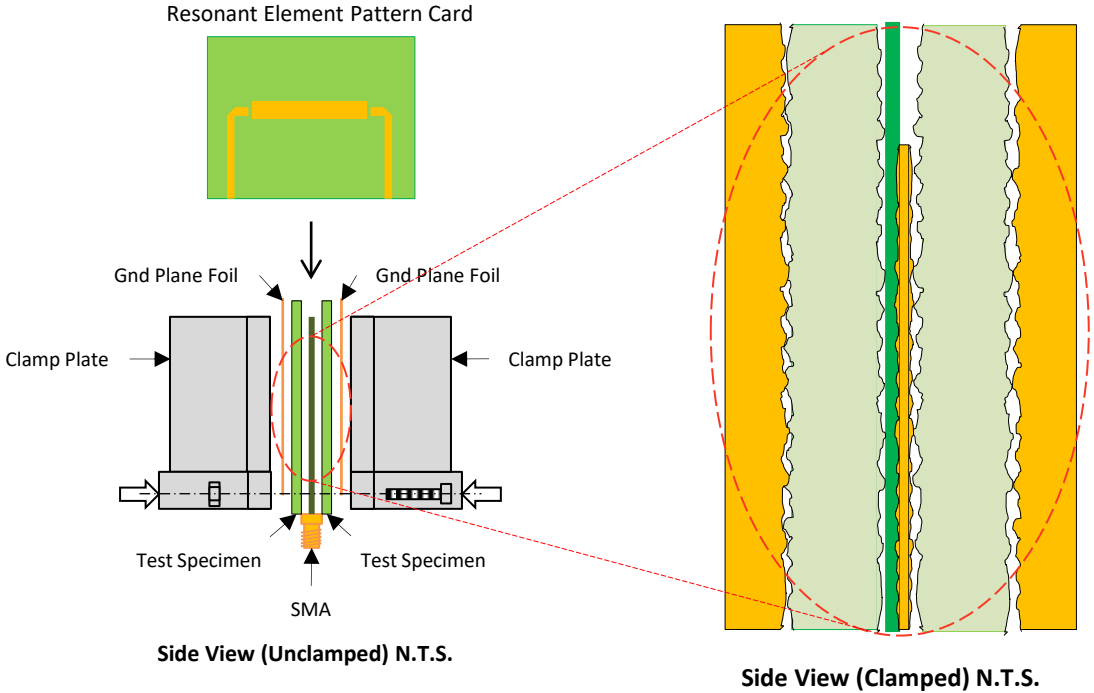


Side View (Unclamped) N.T.S.

IPC-TM-650 test method used to rapidly test dielectric material for permittivity and loss tangent in a production environment

IPC-TM-650 - Section 2.5.5.5 - Rev C - Test Fixture [8]

Issues:



Side View (Unclamped) N.T.S.

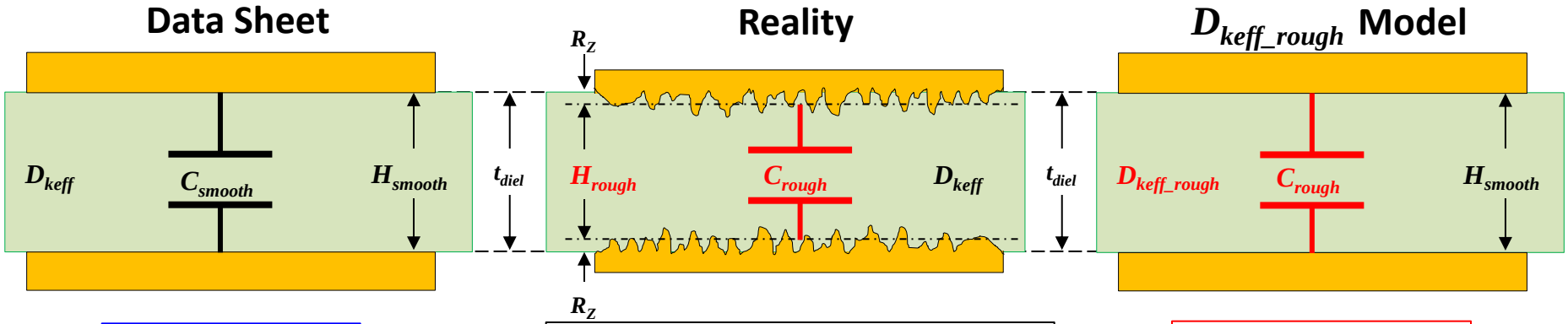
Side View (Clamped) N.T.S.

Since resonant element pattern card & material U.T. not physically bonded together => small air gaps between various layers & conductor roughness affects published results

Published D_k not same as D_{keff} due to roughness

IPC-TM-650 - Section 2.5.5.5 - Rev C - Test Fixture [8]

D_{keff} Due to Roughness Model



$$C_{smooth} = D_{keff}\left(\frac{\varepsilon_0 A}{H_{smooth}}\right)$$

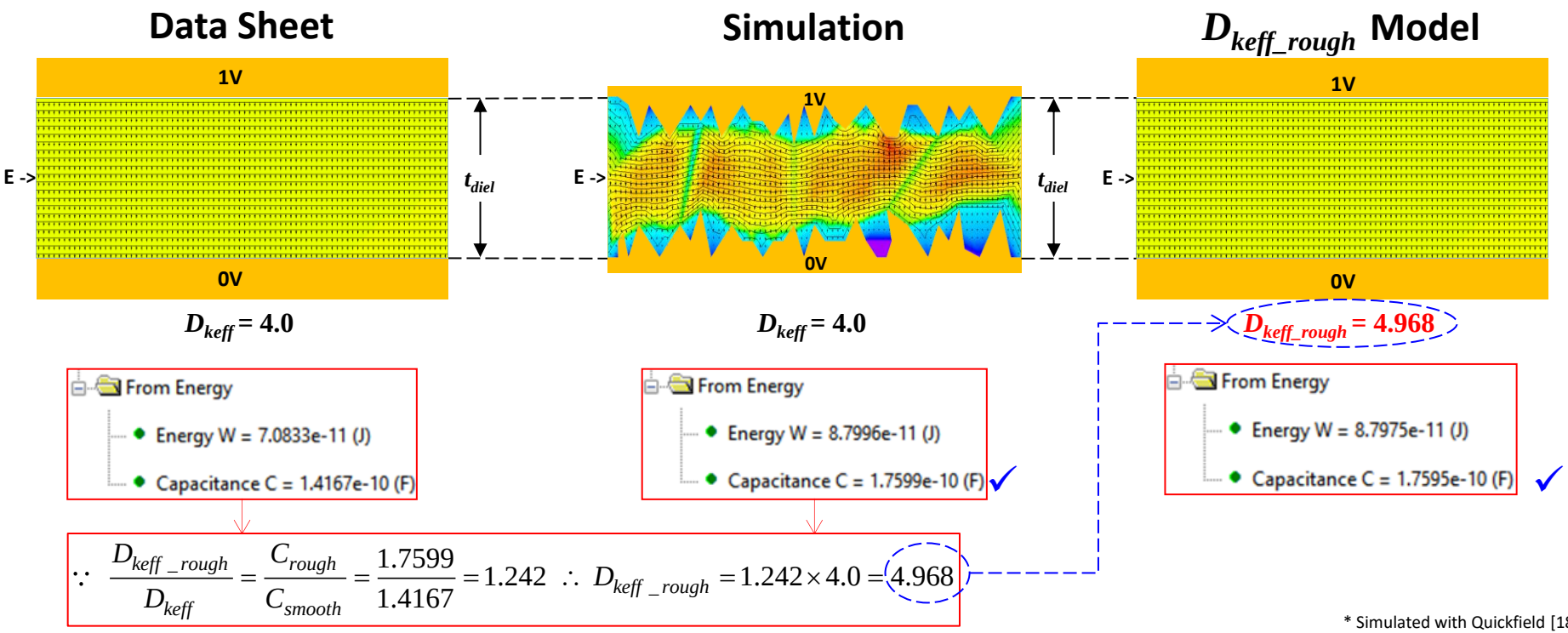
$$C_{rough} = D_{keff}\left(\frac{\varepsilon_0 A}{H_{rough}}\right) = D_{keff}\left(\frac{\varepsilon_0 A}{(H_{smooth} - 2R_z)}\right)$$

$$C_{rough} = D_{keff\_rough}\left(\frac{\varepsilon_0 A}{H_{smooth}}\right)$$

$$\frac{H_{smooth}}{H_{rough}} = \frac{C_{rough}}{C_{smooth}} = \frac{D_{keff\_rough}\left(\frac{\varepsilon_0 A}{H_{smooth}}\right)}{D_{keff}\left(\frac{\varepsilon_0 A}{H_{smooth}}\right)} = \frac{D_{keff\_rough}}{D_{keff}}$$

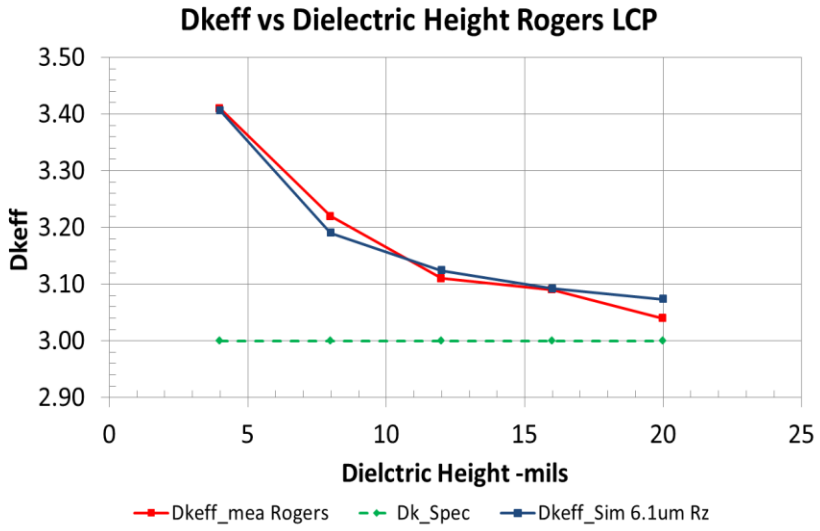
$$D_{keff\_rough} = \frac{H_{smooth}}{(H_{smooth} - 2R_z)} \times D_{keff}$$

Model Validation*



* Simulated with Quickfield [18]

Validating the Model with Rogers Study [3]



$$D_{keff\_rough} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_z\right)} \times D_{keff}$$

1. Tuning R_z equal to 6.1 μm at 4 mil dielectric height
2. Use same value for the other dielectric heights

✓ Excellent correlation to measured D_{keff}

FR408HR/RTF Case Study [10]

CMP-28 Test Platform

Photo courtesy Wild River Technology [11]

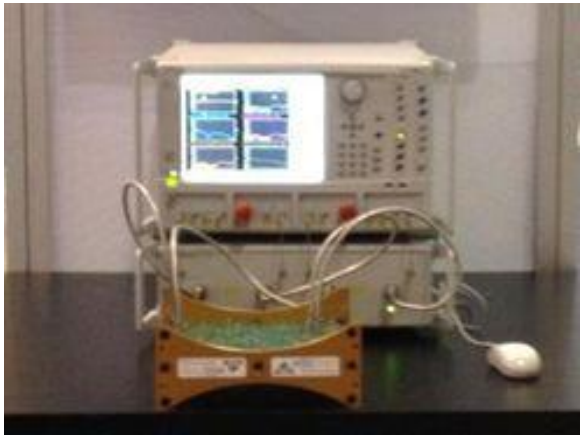
Features:

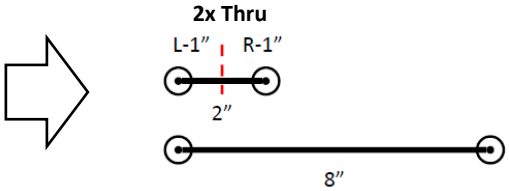
- FR408HR material with reverse-treated foil (RTF)
- Assembled with 2.92mm (CMP-28) or 2.4mm (CMP-32) connectors
- 3D EM benchmark structures
    - Loss structures for material extraction
    - Resonators for measurement correspondence
    - Multi-impedance structures for VNA time transform analysis

Applications:

- 3D-EM and measurement assistance for the SI practitioner
    - Vias
    - Multimode Analysis
    - Meshing Analysis Structure
    - Advanced Material Extraction and Loss Modeling
- THRU Calibration, T-matrix de- embedding
- Advanced Crosstalk analysis
- TRL/LRM Calibration Verification/Benchmark

Measure and De-embed for Generalized Modal S-parameters (GMS)





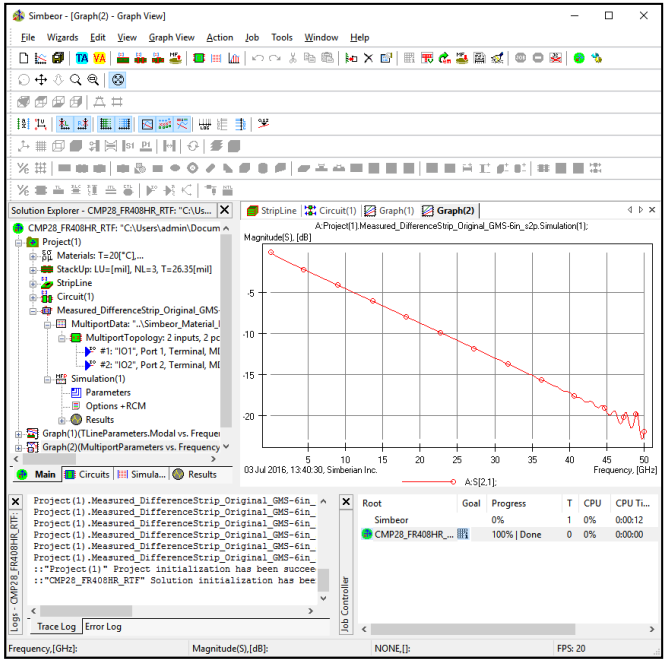
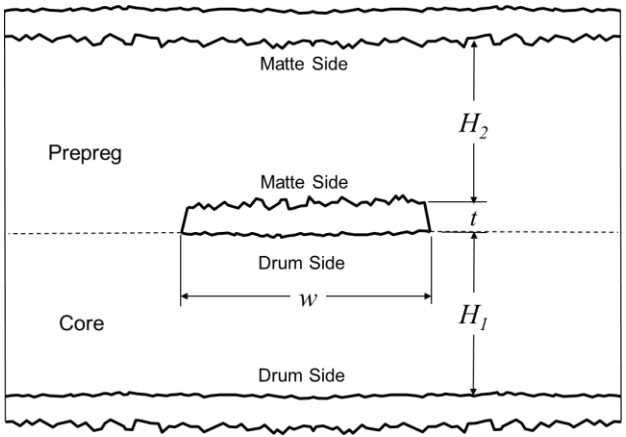


Photo courtesy Anritsu [19]

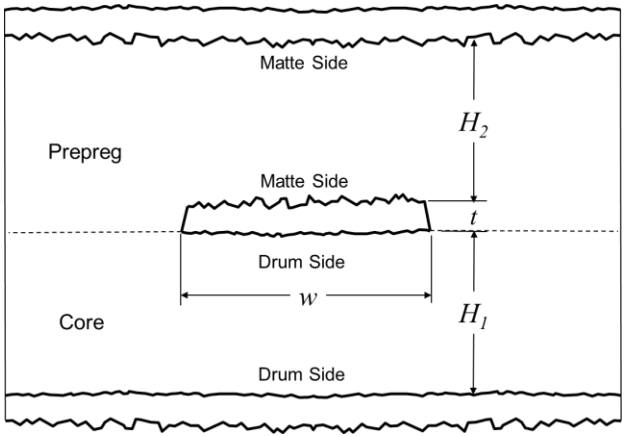
Simulated with Simbeor SW [14]

FR408HR/RTF Data Sheet & Test Board Design Parameters



Parameter	FR408HR/RTF
D_k Core/Prepreg @ f_o	3.65/3.59 @10GHz
D_f Core/Prepreg @ f_o	0.0094/0.0095 @ 10GHz
R_z Drum side	3.048 μm
R_z Before Micro-etch-Matte side	5.715 μm
R_z After 50 μin (1.27 µm) Micro-etch treatment - Matte side	4.445 μm
Trace Thickness, t	1.25 mils (31.73 μm)
Trace Etch Factor	60 deg taper
Trace Width, w	11 mils (279.20 μm)
Core thickness, H1	12 mils (304.60 μm)
Prepreg thickness, H2	10.6 mils (269.00 μm)
De-embedded trace length	6.00 in (15.24 cm)

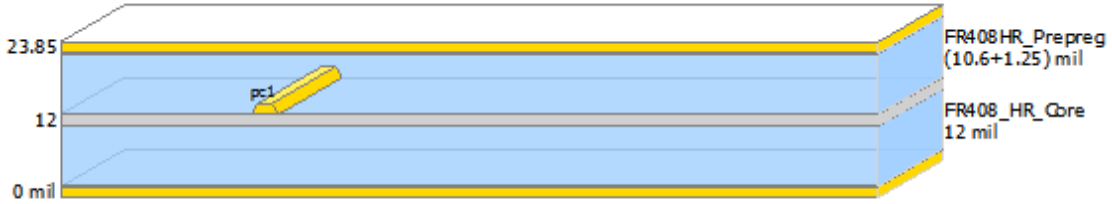
Determine D_{keff} Due to Roughness Core/Prepreg

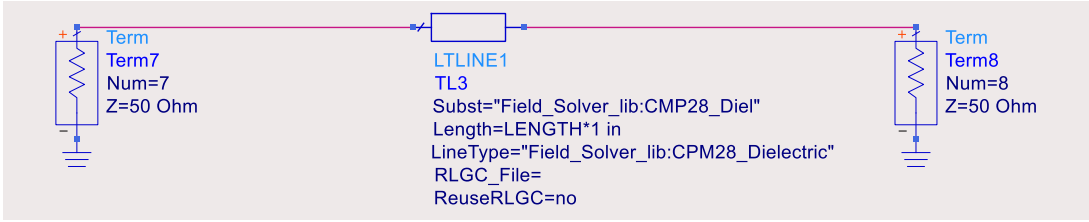


$$D_{keff\_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_z\right)} \times D_{k\_prepreg} = \frac{269\mu m}{\left(269\mu m - 2\times 4.445\mu m\right)} \times 3.59 = 3.713$$

$$D_{keff\_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_z\right)} \times D_{k\_core} = \frac{304.6\mu m}{\left(304.6\mu m - 2\times 3.048\mu m\right)} \times 3.65 = 3.725$$

Determine Dielectric Loss

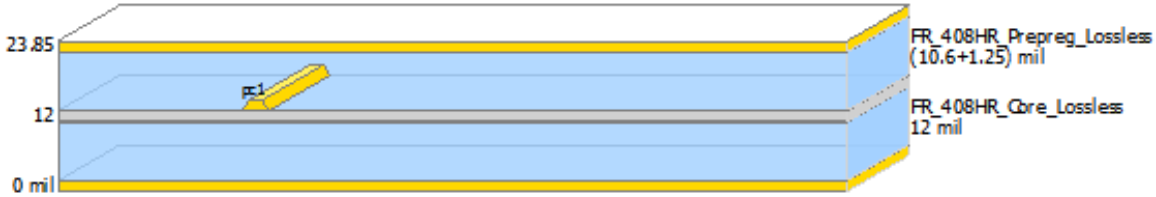


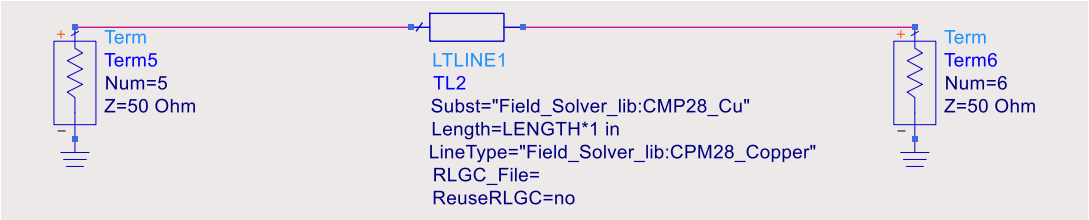


- ✓ Set Conductivity Cu to 5.8E17 S/m (lossless)
- ✓ Svensson/Djordjevic Causal loss model
- ✓ D_{keff} / D_f values @10GHz for core/prepreg

Keysight ADS – [6]

Determine Smooth Conductor Insertion Loss

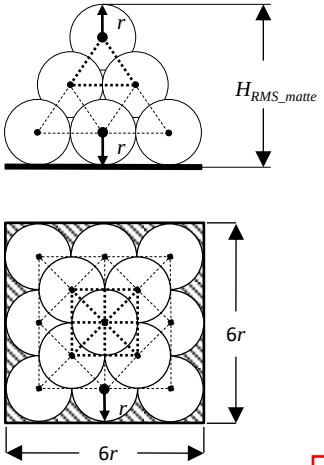




- ✓ Set D_f to 0 (Lossless)
- ✓ Set Conductivity 5.8E7 s/m

Keysight ADS – [6]

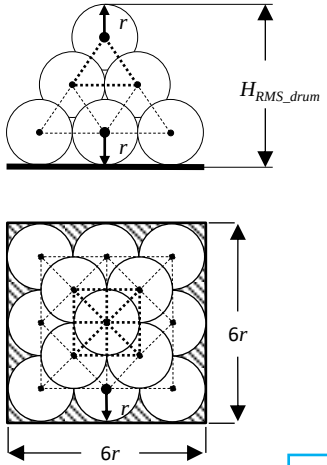
Determine Matte & Drum Correction Factors [10]



$$r_{matte} = \frac{H_{RMS\_matte}}{2\left(1+\sqrt{2}\right)}$$

$$A_{Flat\_matte} = \left(6r_{matte}\right)^2$$

$$K_{SR\_matte}(f) \approx 1+84\left(\frac{\left(\frac{\pi\left(r_{matte}\right)^2}{A_{Flat\_matte}}\right)}{\left(1+\frac{\delta(f)}{r_{matte}}+\frac{\delta^2(f)}{2\left(r_{matte}\right)^2}\right)}\right)$$



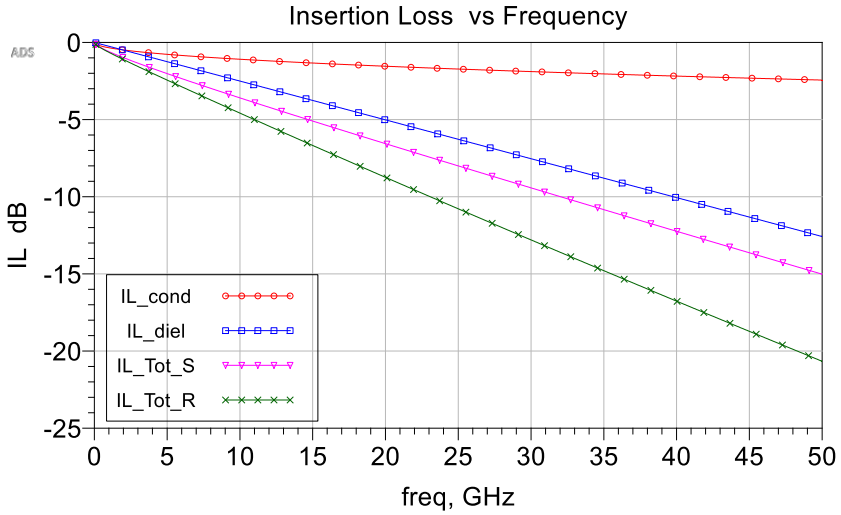
$$r_{drum} = \frac{H_{RMS\_drum}}{2\left(1+\sqrt{2}\right)}$$

$$A_{Flat\_drum} = \left(6r_{drum}\right)^2$$

$$K_{SR\_drum}(f) \approx 1+84\left(\frac{\left(\frac{\pi\left(r_{drum}\right)^2}{A_{Flat\_drum}}\right)}{\left(1+\frac{\delta(f)}{r_{drum}}+\frac{\delta^2(f)}{2\left(r_{drum}\right)^2}\right)}\right)$$

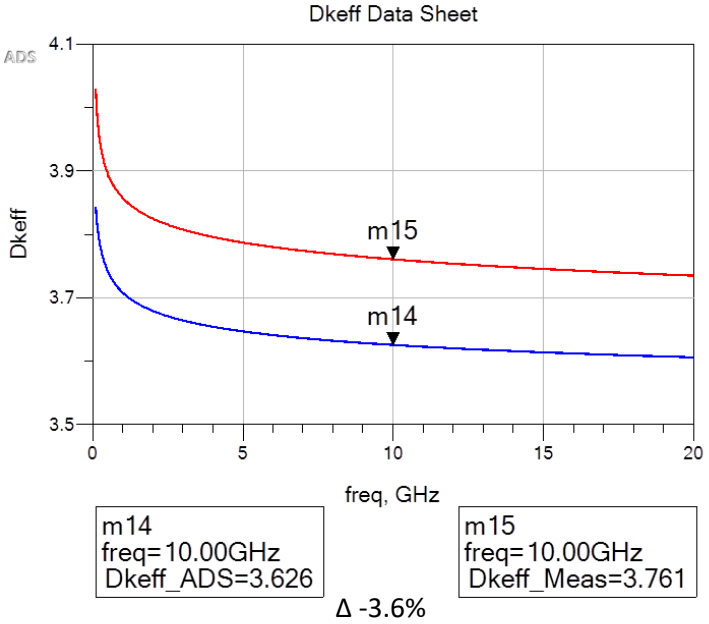
Total IL Due to Surface Roughness

$$IL_{total}(f) = IL_{diel}(f) + 0.5\left(K_{SR\_matte}(f) + K_{SR\_drum}(f)\right) IL_{conductor}(f)$$

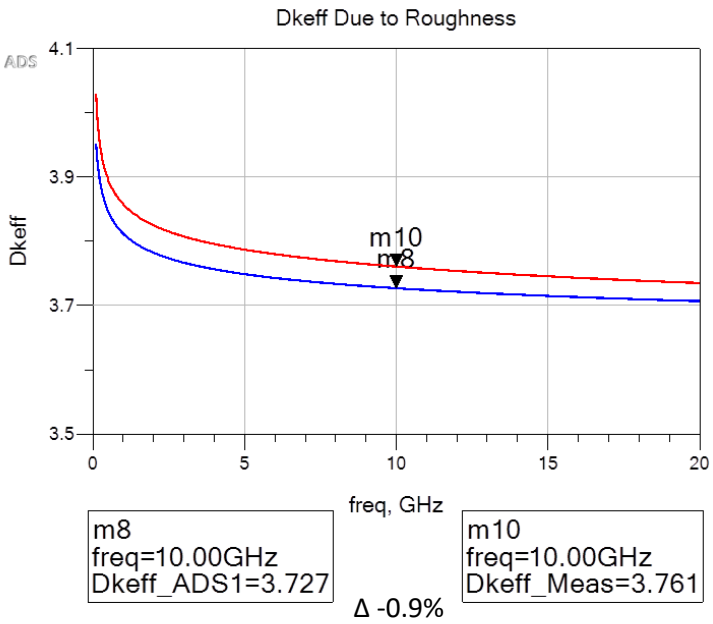


Simulated with Keysight ADS [6]

FR408HR Simulation Results for D_{keff}



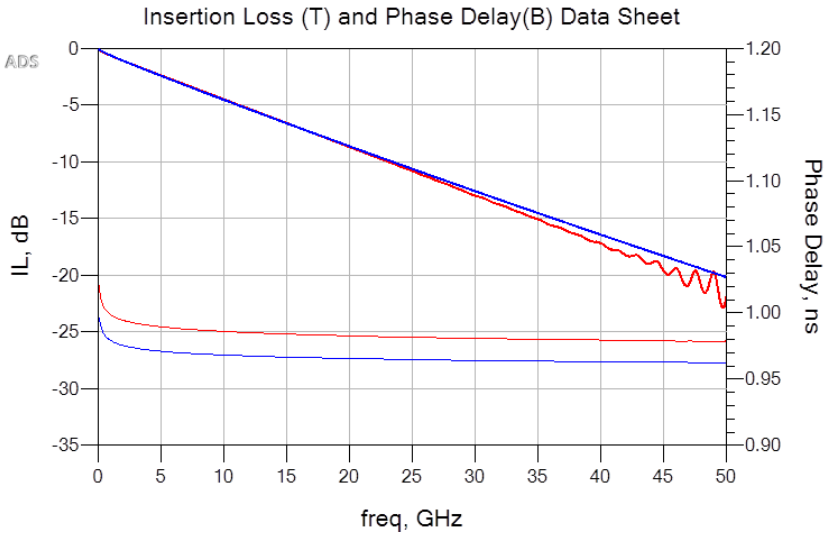
Data Sheet Values



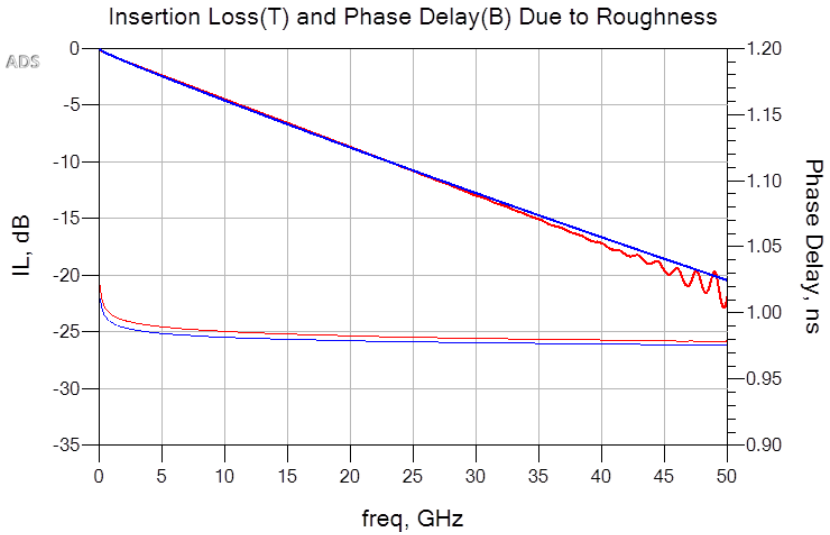
D_{keff} Roughness Model

Simulated with Keysight ADS [6]

FR408HR Simulation Results for IL & Phase Delay



Data Sheet Values

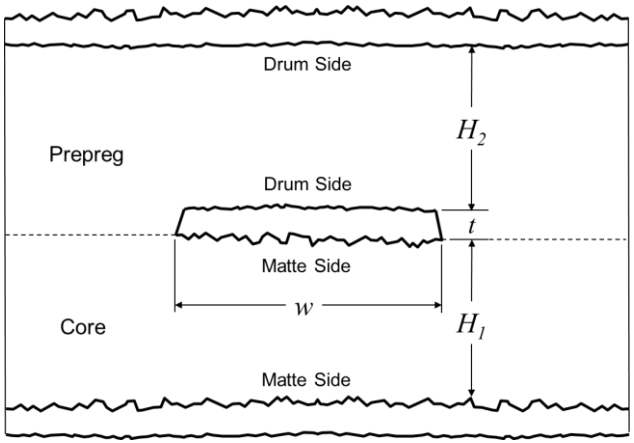


D_{keff} Roughness Model

Simulated with Keysight ADS [6]

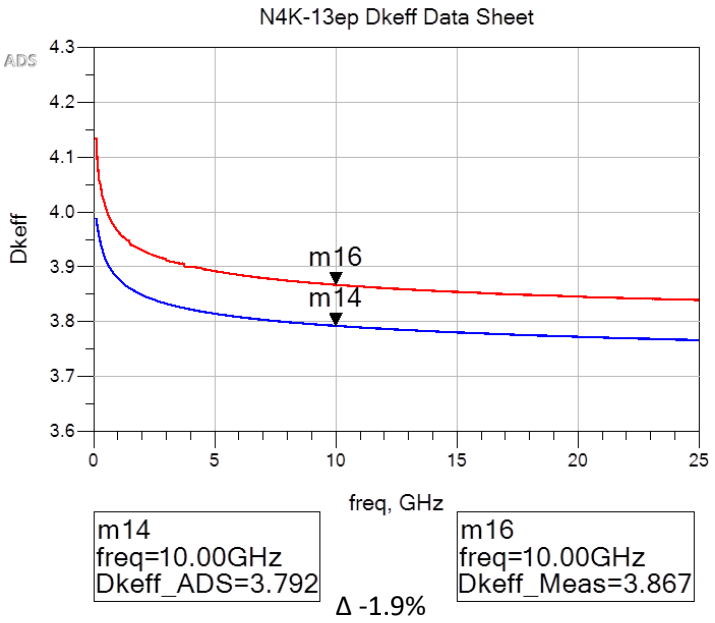
N4000-13ep/VLP Case Study [9]

N4000-13ep/VLP Data Sheet & Test Board Design Parameters

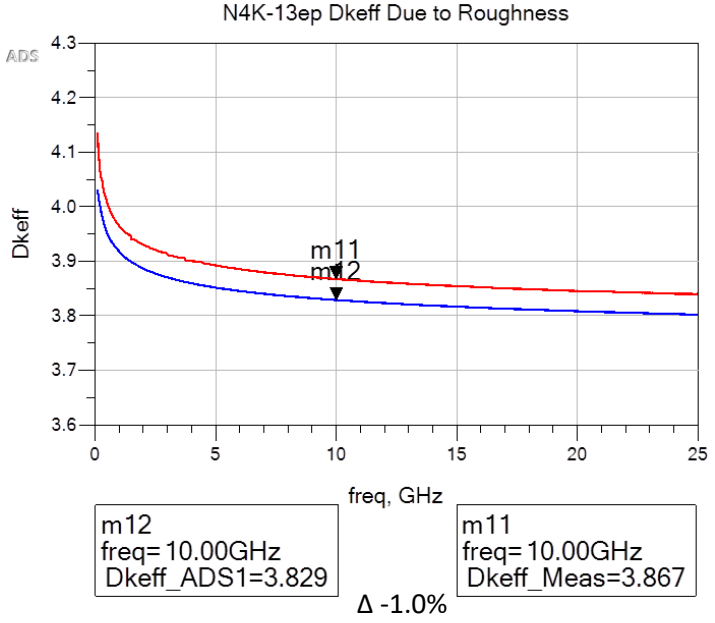


Parameter	N4000-13EP/VLP
D_k *Core/Prepreg*	3.83/3.72 @10GHz
D_f *Core/Prepreg*	0.0085/0.0085 @ 10GHz
R_z Matte side	2.50 μm
R_a Drum w/ Micro-etch	1.44 μm
Trace Thickness, t	15.23 μm
Trace Etch Factor	2:1 (60 deg taper)
Trace Width, w	9.9 mils (251 μm)
Core thickness, H_1	9.8 mils (249 μm)
Prepreg thickness, H_2	9.09 mils (231 μm)
GMS trace length	4 in (10.15cm)

N4000-13ep Simulation Results for D_{keff}



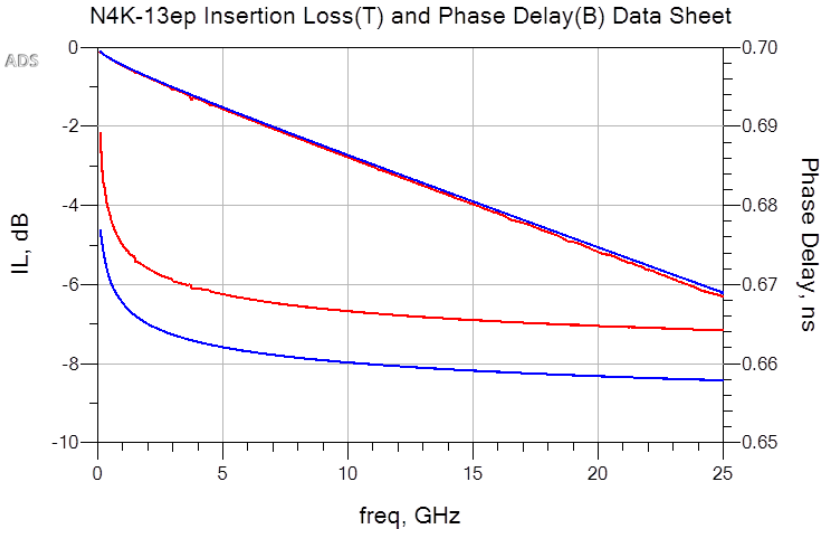
Data Sheet Values



D_{keff} Roughness Model

Simulated with Keysight ADS [6]

N4000-13ep Simulation Results for IL & Phase Delay



Data Sheet Values

D_{keff} Roughness Model

Simulated with Keysight ADS [6]

Summary and Conclusions

1. Analysis supports the theory that surface roughness profile decreases the separation between the reference plane(s) and conductor, thereby increasing the e-field strength, resulting in additional distributed capacitance, which accounts for increased D_{keff} and phase delay as summarized by:

$$\frac{E_{rough}}{E_{smooth}} = \frac{H_{smooth}}{H_{rough}} = \frac{C_{rough}}{C_{smooth}} = \frac{D_{keff\_rough}}{D_{keff\_smooth}} = \frac{TD_{rough}}{TD_{smooth}}$$

2. By using an effective D_k due to roughness derived from Gauss' Law for parallel plate capacitors instead of published D_k values from data sheets yields excellent results when compared to measured data without curve fitting.

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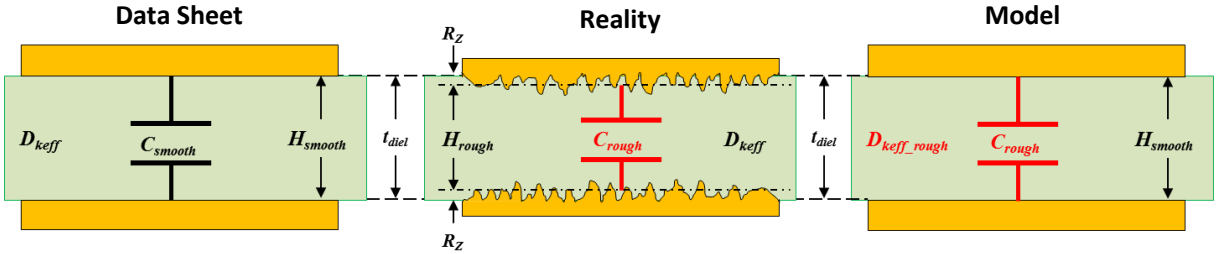
Appendix

Appendix: D_{keff} Due to Roughness Model Derivation



$$C_{smooth} = \frac{D_{keff}\,\varepsilon_0 A}{H_{smooth}}$$

$$C_{rough} = \frac{D_{keff}\,\varepsilon_0 A}{H_{rough}}$$

$$\frac{C_{smooth}}{C_{rough}} = \frac{H_{rough}}{H_{smooth}}$$

$$\therefore H_{rough} = H_{smooth}\,\frac{C_{smooth}}{C_{rough}}$$

$$C_{rough} = \frac{D_{keff}\,\varepsilon_0 A}{H_{rough}} = \frac{D_{keff}\,\varepsilon_0 A}{H_{smooth}\,\dfrac{C_{smooth}}{C_{rough}}} = \frac{\varepsilon_0 A}{H_{smooth}} \times D_{keff}\,\frac{C_{rough}}{C_{smooth}}$$

$$If:$$

$$D_{keff}\,\frac{C_{rough}}{C_{smooth}} = D_{keff\_rough}$$

$$Then:$$

$$C_{rough} = D_{keff\_rough}\,\frac{\varepsilon_0 A}{H_{smooth}}$$

$$\frac{C_{rough}}{C_{smooth}} = \frac{H_{smooth}}{H_{rough}} = \frac{D_{keff\_rough}\,\dfrac{\varepsilon_0 A}{H_{smooth}}}{D_{keff}\,\dfrac{\varepsilon_0 A}{H_{smooth}}} = \frac{D_{keff\_rough}}{D_{keff}}$$

$$\therefore D_{keff\_rough} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_z\right)} \times D_{keff}$$

Thank You!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