

PCB Interconnect Modeling Demystified

This session was presented as part of the DesignCon 2019 Conference and Expo

For more information on the event, please go to DesignCon.com











PCB Interconnect Modeling Demystified

Bert Simonovich

Lamsim Enterprises Inc. Isimonovich @lamsimenterprises.com



DESIGNCON[®] 2019

JAN 29 - 31, 2019



High-level Design Challenges



Choosing appropriate diff pair geometry, board material and stackup to meet insertion loss budgets for industry standards can be overwhelming





Transmission Line Modeling



Important to model dielectric and conductor loss accurately

 $IL_{total}(f) = IL_{diel}(f) + K_{SR}(f) \times IL_{conductor}(f)$



Failure To Model Roughness Can Be Problematic



With just 3.4dB delta @14 GHz => 17% reduction averaged across all 3 eye heights with rough copper @56GB/s





Dielectric Properties



Failure to correct D_k from data sheet due to conductor roughness => inaccuracy in simulated IL & Phase Delay





EDA Tool Challenges

 Many EDA tools include latest and greatest models for conductor surface roughness and wideband dielectric properties



But obtaining the right parameters to feed models is always a challenge



Design Feedback Method



Benefits:

- Practical
- Accurate

Issues:

- Expertise required
- Time
- Money
- Extracted parameters only accurate for sample from which they were extracted



"Sometimes an OK answer NOW! is better than a good answer late...." – Eric Bogatin



What You Will Learn

- How to apply my Cannonball stack model to determine roughness parameters for Huray model from data sheets
- ✓ How to determine D_{keff} due to roughness from data sheets
- ✓ How to apply these parameters in popular field solvers.
- ✓ Impact of causal metal model to simulated results
- Impact of Oxide/Oxide Alternative treatments on roughness, insertion loss and impedance
- How to pull it all together and compare simulated transmission line interconnect models with case studies





Overview



Current Distribution Through a Conductor





DC current is uniform through cross-sectional area of conductor

AC current above ~10MHz flows mainly along "skin" of the conductor





Conductor Roughness





No such thing as a perfectly smooth PCB conductor surface

Roughness is always applied to promote adhesion to the dielectric material





Copper Foil Manufacturing Processes



- Smoother
- Higher Cost

- Rougher
- Lower Cost





Common ED Roughness Profiles

Standard Profile



IPC Very Low Profile(VLP)



Ultra Low Profile (ULP)Class



No min/max spec

 R_{z} < 5.2 μ m max

-Other names: HVLP, VSP -No IPC spec -Typically R_z < 2 μ m max



ED Copper Foil Nodulation Treatment



Drum Side Untreated



Matte Side Untreated





Drum Side Treated OR



Matte Side Treated

UBM





Oxide/Oxide Alternative Treatment

During PCB fabrication untreated copper on each side of core laminate undergoes a roughening treatment to promote adhesion





Reverse Treated Foil (RTF) After Oxide Alternative Treatment







Roughness Parameters

RMS (R_q) / Average (R_a)











Modeling Conductor Roughness





"All models are wrong but some are useful..." - George E. P. Box



Triangular Roughness Model



If RMS height of triangular profile = Δ , then: $\Delta = \frac{R_z}{2\sqrt{3}}$ Likewise if $\Delta \approx R_q$, then: $R_z \approx R_q (2\sqrt{3})$



Hamerstad & Jensen Model





 $\Delta = RMS$ tooth height in meters



Loses accuracy above ~ 3-15GHz depending on roughness of copper





Huray "snowball" Model



SEM Photo Reference [15]

Based on non-uniform distribution of spheres resembling "snowballs" applied to a matte base

$$K_{SRH}\left(f\right) = \frac{P_{rough}}{P_{flat}} \approx \frac{A_{matte}}{A_{flat}} + \frac{3}{2} \sum_{i=1}^{j} \left(\frac{N_i \times 4\pi a_i^2}{A_{flat}}\right) \left(1 + \frac{\delta(f)}{a_i} + \frac{\delta^2(f)}{2a_i^2}\right)^{-1}$$





Huray Model Prior Art



SEM Photo Reference [15]

Assumes stacked "snowballs" arranged in hexagonal lattice

11 spheres min; 38 spheres max of radius 1μ m to fit within hex tile area and height of 5.8μ m

Fit equation parameters to measured data





Cannonball-Huray Model





Applying Cannonball-Huray Model For Popular EDA Tools

	ΤοοΙ	Parameters				
•	Polar Si9000e [5]; Mentor Hyperlynx [19] include the Cannonball-Huray model as an option	R _Z				
•	Ansys [25]; Cadence [26] tools require surface ratio (<i>sr</i>) and nodule radius (<i>r</i>) as input parameters	$sr = \left(\frac{14 \times 4\pi r^2}{A_{flat}}\right) = \left(\frac{14 \times 4\pi r^2}{36r^2}\right) = 1.56\pi \approx 4.9$ $r \approx 0.06R_{Z}$				
•	Simbeor [22] requires roughness factor (<i>RF</i> 1) and sphere radius (<i>SR</i> 1)	$RF1 = 1 + \frac{3}{2} \left(\frac{N4\pi r^2}{A_{flat}} \right) = 1 + \frac{3}{2} \left(\frac{14 \cdot 4\pi (r_{avg})^2}{36(r_{avg})^2} \right) \approx 8.33$ $SR1 = r \approx 0.06R_{z}$				





Modeling $D_{ke\!f\!f}$ Due to Surface Roughness



Dielectric Material Terms

Complex dielectric constant ε defined as:

$$\mathcal{E} = \mathcal{E}' - j\mathcal{E}'' \qquad \tan(\delta) = \frac{\mathcal{E}'}{\mathcal{E}'}$$

If real part $\varepsilon' = D_k$ and $\tan(\delta) = D_f$ then:

$$D_f = \frac{\varepsilon^{"}}{D_k}$$



 $\delta =$ loss angle



Dk, (Lai Tes

Df.

Marketing Data Sheet Issues

	Typical Values						
Pro	perty			Units	Test Helhod		
		Typical Value	Specification	Metric	IPC-TM-660 (or as noted)		
Glass Transition Temperature (Tg) by DSC	:	200	170-200	°C	2.4.25		
Decomposition Temperature (Td) by TGA	© 5% weight loss	360	and the second second	°C	ASTM D3850		
T260		60	-	Minutes	ASTM D3850		
T288		>30	-	Minutes	ASTM D3850		
CTE, Z-axis	A. Pre-Tg B. Post-Tg	55 230	MBUS -	ppm/%C	2.4.24		
CTE, X-, Y-axes	A. Pre-Tg B. Post-Tg	16 18	ANBUS -	ppm/°C	2.4.24		
Z-axis Expansion (50-260°C)		2.8	-	%	2.4.24		
Thermal Conductivity		0.4	-	W/mK	ASTM D5930		
Thermal Stress 10 sec @ 288°C (550.4°F)	A. Unetched B. Etched	Pass	Pass Visual	Rating	2.4.13.1		
Dk, Permittivity Laminate & prepreg as laminated) Fested at 56% resin	A. @ 100 MHz (HP4285A) B. @ 1 GHz (HP4291A) C. @ 2 GHz (Bereskin Stripline) D. @ 5 GHz (Bereskin Stripline) E. @ 10 GHz (Bereskin Stripline)	3.72 3.69 3.68 3.64 3.65	5.4 - - 		2.5.5.3 2.5.5.5 2.5.5.5 2.5.5.5 2.5.5.5		
Df, Loss Tangent Laminate & prepreg as laminated) Tested at 66% resig	0.0072 0.0091 0.0092 0.0098 0.0095	0.035 - - - -	-	2.5.5.3 2.5.5.9 2.5.5.5 2.5.5.5 2.5.5.5			
A. 96/35/90 B. Atter molsture resistance C. At elevated temperature		4.4x10 ⁷ 9.4x10 ⁷	1.0x10 ⁶ 	MΩ-em	2.5.17.1		
A. 96/35/90 B. After molsture resistance C. At elevated temperature		2.6x10 ⁶ 2.1x10 ⁸	1.0x104 	MΩ	2.5.17.1		
Dielectric Breakdown		>50	-	KV	2.5.6		
Arc Resistance		137	60	Seconds	2.5.1		
Electric Strength (Laminate & prepreg as	laminated)	70 (1741)	30 (750)	kV/mm (V/mil)	2.5.6.2		
Comparative Tracking Index (CTI)		3 (175-249)	-	Class (Volts)	UL-746A ASTM D3638		
Peel Strength	A Low profile copper tail and very tow profile – all copper weights >17 microns B. Standard profile copper 1, After thermal stress 2, At 1267 (26747) 3. After process solutions	1.14 (6.5) 0.96 (5.5) 0.90 (5.1)	1.14 (6.5) 0.70 (4.0) N/mm 0.96 (5.5) 0.80 (4.5) - 0.70 (4.0) 0.90 (5.1) 0.55 (3.0)		2.4.8 2.4.8.2 2.4.8.3 - -		
Flexural Strength	exural Strength A. Lengthwise direction B. Crosswise direction		-	b/inch ²	2.4.4		
Tensile Strength	A Lengthwise direction B. Crosswise direction		-	Ib/Inch ²	-		
Young's Modulus	A. Grain direction B. Fill direction		-	ksi	w		
Poisson's Ratio	A. Grain direction B. Fill direction	0.137 0.133	-	-	x		
Moisture Absorption		0.061	-	%	2.6.2.1		
Flammability (Laminate & prepreg as lam	linated)	V-0	-	Rating	UL 94		
Max Operating Temperature		130	UL Cart	°C	-		
The data, while believed to be accurate and based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the arms and conditions of the agreement under which they are sold.							

Dk, Permittivity (Laminate & prepreg as laminated) Tested at 56% resin	A. @ 100 MHz (HP4285A) B. @ 1 GHz (HP4291A) C. @ 2 GHz (Bereskin Stripline) D. @ 5 GHz (Bereskin Stripline) E. @ 10 GHz (Bereskin Stripline)	3.72 3.69 3.68 3.64 3.65	5.4 - - -	-	2.5.5.3 2.5.5.9 2.5.5.5 2.5.5.5 2.5.5.5 2.5.5.5
Df, Loss Tangent (Laminate & prepreg as laminated) Tested at 56% resin	A. @ 100 MHz (HP4285A) B. @ 1 GHz (HP4291A) C. @ 2 GHz (Bereskin Stripline) D. @ 5 GHz (Bereskin Stripline) E. @ 10 GHz (Bereskin Stripline)	0.0072 0.0091 0.0092 0.0098 0.0095	0.035 - - -	_	2.5.5.3 2.5.5.9 2.5.5.5 2.5.5.5 2.5.5.5 2.5.5.5

Using D_k/D_f numbers from marketing data sheets for stackup and channel modeling will give inaccurate results



Engineering Data Sheets

Core Data

Core	Resin	Thickness (inch)	Thickness	Dielectric Constant(DK) / Dissipation Factor(DF)							
Constructions	Content (%)		(mm)	100 MHz	500 MHz	1.0 GHz	2.0 GHz	5.0 GHz	10.0 GHz	15.0 GHz	20.0 GHz
4 499	72.0	0.0020 ZBC	0.0508 ZBC	3.37	3.36	3.34	3.32	3.30	3.30		
1×106				0.0075	0.0089	0.0096	0.0101	0.0107	0.0107		
4 4997	69.0	0.0025	0.0635	3.42	3.40	3.38	3.36	3.34	3.33		
1X1067				0.0075	0.0084	0.0095	0.0100	0.0105	0.0104		
11999		0.0025	0.0635	3.67	3.64	3.62	3.61	3.60	3.59		
1X1080	57.0			0.0071	0.0079	0.0089	0.0092	0.0097	0.0095		
4:4000	50.0	0.0030	0.0762	3.65	3.63	3.60	3.59	3.57	3.57		
1X1086	58.0			0.0072	0.0079	0.0091	0.0092	0.0098	0.0095		
11000	63.0	0.0030	0.0762	3.54	3.52	3.50	3.48	3.47	3.47		
1X1080				0.0074	0.0082	0.0092	0.0096	0.0102	0.0101		
4-0040	51.0	0.0035	0.0889	3.82	3.79	3.77	3.77	3.74	3.74		
1x3313				0.0068	0.0076	0.0084	0.0087	0.0092	0.0090		
0.400	67.0	0.0035	0.0889	3.46	3.45	3.42	3.40	3.38	3.37		
2×106				0.0074	0.0083	0.0094	0.0098	0.0104	0.0102		
400/4000	59.0	0.0040	0.1016	3.63	3.61	3.58	3.57	3.55	3.54		
106/1080				0.0072	0.0080	0.0090	0.0093	0.0098	0.0096		
1.0010	55.0	55.0 0.0040	0.1016	3.72	3.70	3.68	3.66	3.65	3.65		
1X3313				0.0071	0.0077	0.0087	0.0090	0.0095	0.0094		
400/4000	61.0	0.0043	0.1092	3.57	3.56	3.54	3.52	3.51	3.50		
106/1080				0.0073	0.0081	0.0092	0.0095	0.0099	0.0098		
2:4007	63.0	0.0043	0.1092	3.54	3.52	3.50	3.48	3.47	3.47		
2×1007				0.0074	0.0082	0.0092	0.0096	0.0102	0.0101		
106/1000	62.0	0.0045	0.1143	3.55	3.54	3.52	3.50	3.48	3.48		
100/1080	62.0			0.0073	0.0082	0.0092	0.0095	0.0100	0.0098		

Provides:

- ✓ Actual core/prepreg thicknesses
- ✓ Resin content

✓ $D_k(f) / D_f(f)$ for different glass styles





Causal Dielectric Model

Because Complex Dk has real and imaginary components => Causal Dielectric model



Most EDA tools include wideband Debye model

-Input $D_k(f) / D_f(f)$ at a single frequency near Nyquist of baud rate





Dielectric Modeling Issue



When Data Sheet D_k is not the same as Effective D_k



IPC-TM-650 Clamped Stripline Resonator Test Method



Issue:

Since resonant element pattern card & material U.T. not physically bonded together => small air gaps between various layers & conductor roughness affects published results

Published D_k not same as D_{keff} due to roughness

Side View (Clamped) N.T.S.





$D_{ke\!f\!f}$ Due to Roughness Model





FR408HR/RTF Simulation Results for D_{keff}



0

UBM


Causal Roughness Correction Factors





FR408HR/RTF Simulation Results for D_{keff}



 D_{keff} corrected due to roughness and complex roughness correction factor applied

✓ Excellent Results!





HDPUG Oxide Alternative Study Results



In 2016 the High-density Packaging User Group (HDPUG) [16] undertook a project to evaluate the high frequency loss impacts of a variety of OA treatments on a Megtron-6 (Meg-6) test platform using HVLP base foil on core laminates prior to lamination.



Typical Etch vs Non-Etch OA Treatments



Etch Samples A, B, C Non-etch Samples D, E, F



H1

Er1

H2

Er2

W1

W2

S1

T1

3.9000

3.4856

5.6000

3.2541

4.5000

4.0000

8.0000

0.6000

2.7000

97.70



Impact of Oxide Alternative Case Study

Megtron-6 / HVLP Foil 4.5-8-4.5 Geometry



Sample	$OA R_q^*$	OA R_z^{**}	Matte R _z	D _{keff} Core	D _{keff} Prepreg	D_f				
	(µm)	(µm)	(µm)	@12GHz	@12GHz	@12GHz				
Base CU	0.3050	1.0566	1.5000	3.4856	3.2541	0.004				
Α	0.5470	1.8949	1.5000	3.4856	3.2984	0.004				
В	0.5480	1.8983	1.5000	3.4856	3.2986	0.004				
С	0.4400	1.5242	1.5000	3.4856	3.2787	0.004				
D	0.2860	0.9907	1.5000	3.4856	3.2507	0.004				
Ε	0.3170	1.0981	1.5000	3.4856	3.2563	0.004				
F	0.3130	1.0843	1.5000	3.4856	3.2556	0.004				
* Rq data reference	* Rq data reference [17]; ** $R_z \approx R_q (2\sqrt{3})$									

Impact of Oxide Alternative on IL & Impedance

Megtron-6 / HVLP Foil 4.5-8-4.5 Geometry



DESIGNCON[®] 2019

Differential Impedance	Zdiff	97.70
Separation Region Dielectric	REr	2.7000
Trace Thickness	T1	0.6000
Trace Separation	S1	8.0000
Upper Trace Width	W2	4.0000
Lower Trace Width	W1	4.5000
Substrate 2 Dielectric	Er2	3.2541
Substrate 2 Height	H2	5.6000
Substrate 1 Dielectric	Er1	3.4856
Substrate 1 Height	H1	3.9000

JAN 29 - 31, 2019

- 0.07 dB/inch delta between OA sample B and sample D @14GHz 0.16dB/inch delta @ 28GHz
- May not be an issue for 56GB but may be for future 112G depending on interface



time, psec





Model Validation Case Studies





Megtron-4 RTF Case Study



Features:

- Megtron-4
- 1067 Core/prepreg
- 1⁄2 oz RTF
- 1"; 6"; 5"; Diff pairs





ONº 2019

ETS THE BOARD

DESIGN

Parameter	Value		
D_k Core/Prepreg @ 10GHz	3.55/3.41		
D_f Core/Prepreg @ 10GHz	0.008/0.008		
R_z Drum side	2.5 <i>µ</i> m		
R_z Before Micro-etch-Matte side	3.4 <i>µ</i> m		
R_z After 50 μ in (1.27 μ m) Micro-etch treatment -Matte side	2.13 <i>µ</i> m		
Trace Thickness, <i>t</i>	0.63 mils (31.73 <i>µ</i> m)		
Trace Width Base (W_l)	3.5 mils (88.9 μm)		
Trace Width Top (W_2)	3 mils (76.2 μm)		
Space (s)	4.5 mils (114.3 μm)		
Core thickness, H_1	3.9 mils (99.06 μm)		
Prepreg thickness, H_2	3.95 mils (100.33 μm)		
De-embedded trace length	5.00 in (15.24 cm)		

4 1

UBM



Determine D_{keff} Due to Roughness Core/Prepreg



$$D_{keff_prepreg} = \frac{H_2}{(H_2 - 2R_z)} D_{k2} = \frac{100.33\,\mu m}{(100.33\,\mu m - 2(2.13\,\mu m))} \times 3.41 = 3.56$$
$$D_{keff_Core} = \frac{H_1}{(H_1 - 2R_z)} D_{k1} = \frac{99.06\,\mu m}{(99.06\,\mu m - 2(2.5\,\mu m))} \times 3.55 = 3.74$$



Determine Sphere Radius (r) & Base Area (A_{flat})



Drum-side

UBM



~

Input Design Parameters Polar Si9000e





Simulated vs Measured Non-causal Metal Model





DESIGNCON[®] 2019



✓ Excellent Correlation!

UBM



Meg-4/RTF Case Study Single Bit Response and TDR



51











ExaMax Demonstrator Platform



- Design Intent 28 GB/s NRZ
- Meg 6 or N4000-13EPSI Options
 - Nelco N4000-13EPSI Version Used
- MW-G-VSP ¹/₂ oz. foil (VLP)
- 2.9 mm coax connectors
- Case 1 = 8.25" (20.25") L12
- Case 2 = 14.80" (26.8") L10
- Case 3 = 20.22" (32.22") L10
- Case 4 = 26.70" (38.70") L12



Topology Model N4000-13EPSI Summary





K-conn (2.92mm)



Pr

JAN 29 - 31, 2019

MITSUI

Data Sheet Parameters

ELECTROCHE CAL CORP

N4000-13 SI[®] / N4000-13EP SI[®] – Dielectric Properties Table

	Thickness	8	Tol.		Construction	RC%		2GH	lz Dk	2	GH	lz Df	10	GH	łz Dk	10	GH	Hz Df
	0.0020 0.0020 0.0025 0.0030 0.0025 0.0030 0.0035	* * * * * * *	0.0005 0.0005 0.0005 0.0005 0.0005 0.0005 0.0005	1 1 1 1 1 1 1	106 1035 1078 1078 1080 1080 2013	69% 67% 58% 64% 58% 64% 58%	3.04 3.07 3.19 3.11 3.19 3.11 3.29	* * * * * * *	0.056 0.024 0.037 0.020 0.048 0.029 0.027	0.0082 0.0081 0.0077 0.0079 0.0077 0.0079 0.0079	* * * * * * *	0.00021 0.00009 0.00014 0.00007 0.00018 0.00011 0.00010	3.02 3.04 3.16 3.08 3.16 3.08 3.27	± ± ± ± ± ±	0.055 0.024 0.037 0.020 0.048 0.029 0.027	0.0086 0.0085 0.0080 0.0083 0.0080 0.0083 0.0083	* * * * * * *	0.00023 0.00010 0.00016 0.00008 0.00020 0.00012 0.00011
DC Core	0.0040 0.0040 0.0040 0.0050 0.0050 0.0050 0.0060	± ± ± ± ± ±	0.0005 0.0005 0.0005 0.0007 0.0007 0.0007	2 1 1 2 2 2	1035 2013 2116 2116 1078 1078	67% 57% 45% 56% 58% 64%	3.07 3.19 3.38 3.21 3.19 3.11 2.19	* * * * * *	0.010 0.012 0.029 0.001 0.015 0.004 0.026	0.0081 0.0076 0.0069 0.0076 0.0077 0.0079	± ± ± ± ± ±	0.00004 0.00005 0.00011 0.00000 0.00006 0.00002 0.00002	3.04 3.17 3.35 3.18 3.16 3.08 2.16	± ± ± ± ± ±	0.010 0.012 0.029 0.001 0.015 0.004 0.026	0.0085 0.0079 0.0072 0.0079 0.0080 0.0080 0.0083	* * * * * *	0.00004 0.00005 0.00012 0.00001 0.00006 0.00002 0.00011
BP Core	0.0060	± ±	0.0007	2	1080 2013	64% 50%	3.11 3.29	±	0.013	0.0079	±	0.00005	3.08	±	0.013	0.0083	±	0.00006

	Glass	RC%	2 GHz Dk	2GHz Df	10GHz Dk	10GHz Df	Thickness (inches)
	106	75	2.98	0.0084	2.95	0.0088	0.0025
	1035	75	2.98	0.0084	2.95	0.0088	0.0030
BP/DC	1078	65	3.09	0.0080	3.06	0.0084	0.0032
	1080	65	3.09	0.0080	3.06	0.0084	0.0032
Prepreg	2013	58	3.18	0.0077	3.15	0.0080	0.0044
	2116	55	3.22	0.0075	3.19	0.0078	0.0052

Tensile Rz (µm) Elogation eel Strengt μm Strength (%) (kg/cm) (N/mm2) 18 2.5 350 8 1.0 2.5 MW-G-VSP 35 350 16 1.3 70 2.5 350 19 1.5

> ※表中の数値は代表値です。保証値ではありません。 This is representative date, not guarantee.

Performance Copper Foils

ラミ面/Laminate side

OAK-MITSUI

MW-G-VSP

MITSUI KINZOKU CORPORATE GROUP







ExaMax Demonstrator Platform Data Sheet Design Parameters Summary

JAN 29 - 31, 2019



ON 2019

Parameter	N4000-13EPSI Backplane	N4000-13EPSI Daughter Card			
D_k Core/Prepreg @ $10GHz$	3.08/3.06	3.04/3.06			
D_f Core/Prepreg @ $10GHz$	0.0083/0.0084	0.0085/0.0084			
R_z Matte side	2.5 μm	2.5µm			
R_z Drum side w/OA**	1.5 μm	1.5 μm			
Trace Thickness, t	0.6 mils	0.6 mils			
Trace Width, w ₁	6.3 mils	4.9 mils (Diff) 5.4 mils (SE)			
Trace Width, w_2	5.7 mils	4.3 mils (Diff) 4.8 mils (SE)			
Trace Separation, s	5.7 mils	6.1 mils			
Core thickness, H1	6 mils	4 mils			
Prepreg thickness, H2	6.2 mils	6.2mils			

4 h

UBM



Determine D_{keff} Due to Roughness Core/Prepreg





UBM

Determine Sphere Radius (r) & Base Area (A_{flat})



Matte-side



Polar ExaMax Daughter Card SE Trace Parameters





Polar ExaMax Daughter Card Diff Trace Parameters





Polar ExaMax Backplane Diff Trace Parameters



^{**}Length of Line (LL) Adjusted for 8.25"; 14.80"; 20.22"; 26.70"



Generic Topology Model





ExaMax Backplane Case 1 Total Length = 20.25"





ExaMax Backplane Case 2 Total Length = 26.80"





ExaMax Backplane Case 3 Total Length = 32.22"





ExaMax Backplane Case 4 Total Length = 38.70"



---- Measured ---- Simulated



Generic Channel Model





Channel Simulation 53.12 GB/s Case 1 20.25"



Near-end

Far-end

H.

UBM



Summary

- By using dielectric material properties, copper foil and oxide alternative roughness parameters obtained solely from manufacturers' data sheets, a practical method of modeling high-speed differential channels is now achievable using commercial field-solving software employing Huray model.
- ✓ Even though some models are wrong, they can still be useful for getting that answer now rather than later.



References:

- [1] B. Simonovich, "A Practical Method to Model Effective Permittivity and Phase Delay Due to Conductor Surface Roughness". DesignCon 2017, Proceedings, Santa Clara, CA, 2017
- [2] L. Simonovich, "Practical method for modeling conductor roughness using cubic close-packing of equal spheres," 2016 IEEE International Symposium on Electromagnetic Compatibility (EMC), Ottawa, ON, 2016, pp. 917-920. doi: 10.1109/ISEMC.2016.7571773.
- [3] Hammerstad, E.; Jensen, O., "Accurate Models for Microstrip Computer-Aided Design," Microwave symposium Digest, 1980 IEEE MTT-S International , vol., no., pp.407,409, 28-30 May 1980 doi: 10.1109/MWSYM.1980.1124303
- [4] Huray, P. G. (2009) "The Foundations of Signal Integrity", John Wiley & Sons, Inc., Hoboken, NJ, USA., 2009
- [5] Polar Instruments Si9000e [computer software] Version 2017, https://www.polarinstruments.com/index.html,
- [6] Keysight Advanced Design System (ADS) [computer software], (Version 2017). URL: http://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=US&lc=eng.
- [7] Panasonic Industrial Devices and Solutions Division, URL: https://industrial.panasonic.com/ww
- [8] Park Electrochemical Corp. Nelco Digital Electronic Materials, http://www.parkelectro.com/
- [9] Oak-mitsui 80 First St, Hoosick Falls, NY, 12090. URL: http://www.oakmitsui.com/pages/company/company.asp
- [10] Isola Group S.a.r.l., 3100 West Ray Road, Suite 301, Chandler, AZ 85226. URL: http://www.isola-group.com/
- [11] Electrochemicals Inc. CO-BRA BOND®. URL: http://www.electrochemicals.com/ecframe.html
- [12] Macdermid Inc., Multibond. URL: https://electronics.macdermidenthone.com/products-and-applications/printed-circuit-board/surface-treatments/innerlayer-bonding
- [13] Wild River Technology LLC 8311 SW Charlotte Drive Beaverton, OR 97007. URL: http://wildrivertech.com/home/
- [14] IPC-TM-650, 2.5.5.5, Rev C, Test Methods Manual, "Stripline Test for Permittivity and Loss Tangent (Dielectric Constant and Dissipation Factor) at X-Band", 1998
- [15] Stephen H. Hall; Howard L. Heck. (2009). Advanced signal integrity for high-speed digital designs. Hoboken, N.J.: Wiley. pp. 331–336. ISBN 0-470-19235-6
- [16] High Density Packaging User Group International Inc. URL: http://hdpug.org/smooth-copper-signal-integrity
- [17] J. Fuller; K. Sauter, "The Impact of New Generation Chemical Treatment Systems on High Frequency Signal Integrity", IPC APEX 2017 URL: http://hdpug.org/public/hdp-user-group-published-papers-and-presentations/smooth-copper-signal-integrity-paper
- [18] Ciena Corporation, 7035 Ridge Road Hanover, Maryland 21076
- [19] Mentor Hyperlynx [computer software] URL: https://www.mentor.com/pcb/hyperlynx/
- [20] E. Bogatin, D. DeGroot, P.G. Huray, Y.Shlepnev, "Which one is better? Comparing Options to Describe Frequency Dependent Losses," DesignCon 2013, vol. 1, 2013, pp. 469-494 V.
- [21] V. Dmitriev-Zdorov, B. Simonovich, Igor Kochikov, "A Causal Conductor Roughness Model and its Effect on Transmission Line Characteristics", DesignCon 2018 Proceedings, Santa Clara, CA, 2018
- [22] Simberian Inc., 2629 Townsgate Rd., Suite 235, Westlake Village, CA 91361, USA, URL: http://www.simberian.com/
- [23] Amphenol Information, Communications and Commercial (ICC) Division, URL: https://www.amphenol-icc.com/
- [24] E. Bogatin, "Signal Integrity Simplified", Prentice Hall PTR, 2004
- [25] ANSYS Inc., [computer software], URL: https://www.ansys.com/
- [26] Cadence Design Systems Limited, [computer software], URL: https://www.cadence.com/
- [27] IEEE Standard for Ethernet Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation," in IEEE Std 802.3bs-2017 (Amendment to IEEE 802.3-2015 as amended by IEEE's 802.3bw-2015, 802.3by-2016, 802.3bp-2016, 802.3bp-2016, 802.3bp-2016, 802.3bp-2016, 802.3bp-2016, 802.3bp-2016, 802.3br-2016, 802.3br-2017, and IEEE 802.3-2015/Cor1-2017), vol., no., pp.1-372, 12 Dec. 2017 doi: 10.1109/IEEESTD.2017.8207825.
- [28] Isola Group, "Copper Foil 102" Presentation, 2012
- [29] J. A. Marshall, "Measuring Copper Surface Roughness for High Speed Applications", URL: https://electronics.macdermidenthone.com/application/files/3114/9865/4440/Measuring_Copper_Surface_Roughness_for_High_Speed_Applications_IPC_EXpo_2015_Marshall.pdf





Acknowledgements

Hugues Tournier – Ciena Corporation

Heesoo Lee – Keysight Technologies

UBM





Thank You!

Lamsimenterprises.com