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# Relative Permittivity Variation Surrounding PCB Via Hole Structures

SPI2008 Avignon France

May 12-15, 2008

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**NORTEL**



# Introduction

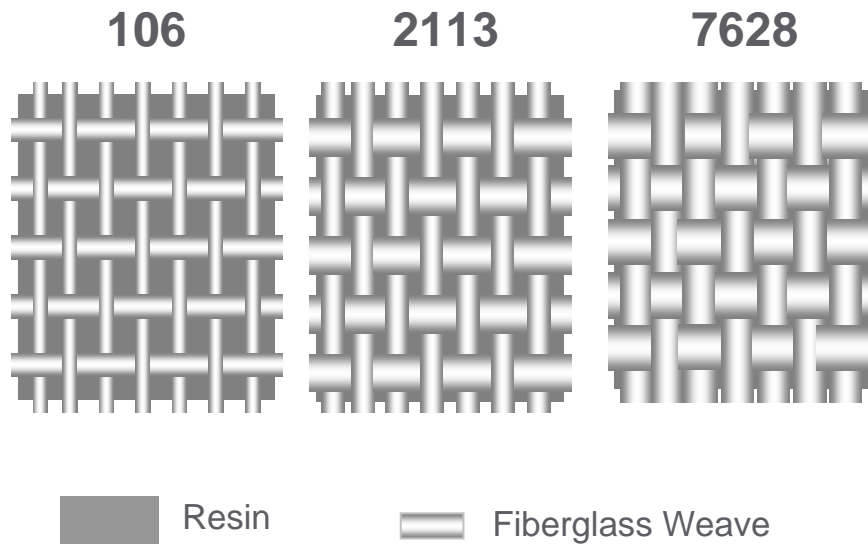
- Present IC technology advancements are allowing data rates beyond 6 Gb/s
- PCB through hole via parasitics becoming more of a factor affecting BER performance
- Accurate via modeling and topology simulation are a must
- All models and methodologies require defining relative permittivity ( $\epsilon_r$ ) or dielectric constant ( $Dk$ ) of material surrounding the via hole structure



# PCB Fabrication Overview

- Conventional PCB laminates are fabricated with a weave of E-glass fiber yarns ( $Dk\ 6.6\ @\ 1MHz$ ) and resin ( $Dk\ 3.2\ @\ 1MHz$ ) [1]
- Effective  $Dk$  is a function of glass to resin ratio of laminates used in the PCB stackup
- For FR-4 PCBs an effective  $Dk$  of 4.3 is often used for trace etch impedance calculations

# Fiberglass Weave vs Resin Content

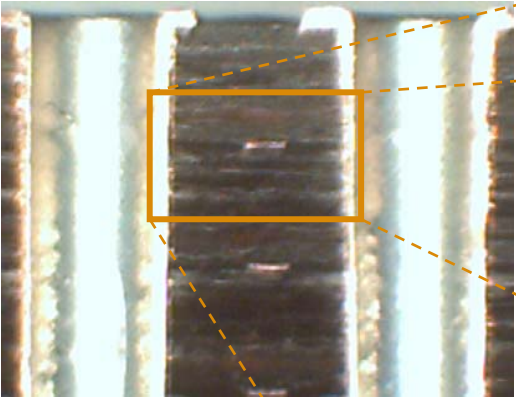


Fiberglass weaves vs. resin content illustration. Smaller glass diameter and thread count results in higher resin content, while larger glass diameter and thread count results in lower resin content.

N4000-6™ Dielectric Properties Table [1], [2]

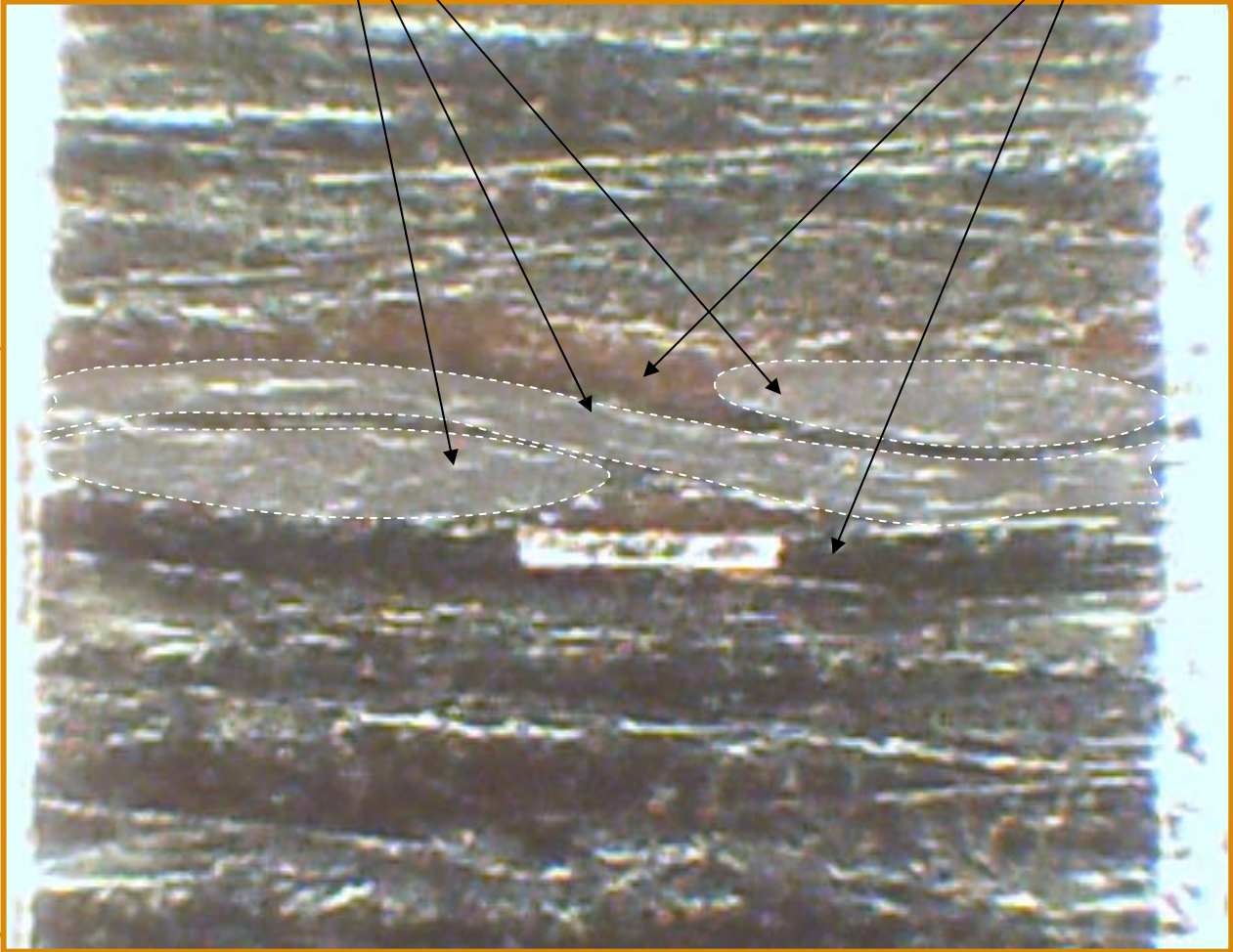
Style	Glass / Laminate Thickness Ratio (mils)	Resin Content (%)	Yarn Count (threads/inch)	Yarn Pitch (mils)
106	1.4/2.0	69.0	56x56	17.9x17.9
1080	2.3/3.0	62.0	60x40	16.7x21.3
2113	2.9/4.0	54.5	60x56	16.7x17.9
2116	3.8/4.0	43.0	60x58	16.7x17.2
7628	6.8/8.0	44.4	44x32	22.7x31.3

# Dielectric Property Between Vias



Via 1

Via 2



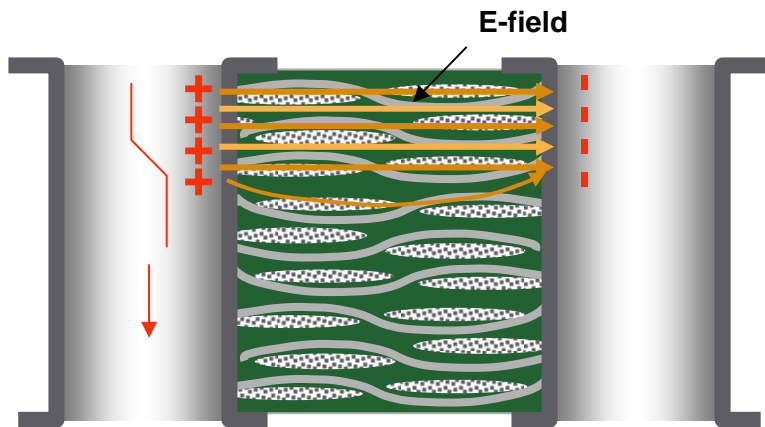
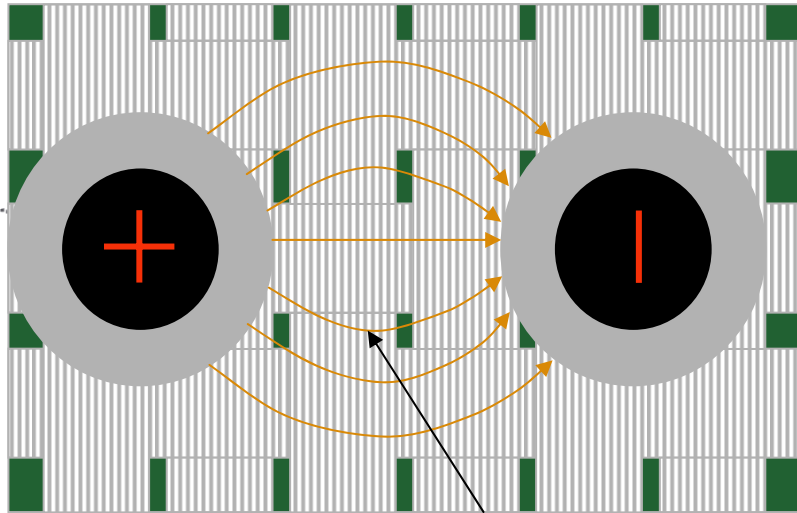
*Fiberglass  
Warp/Fill*

Resin



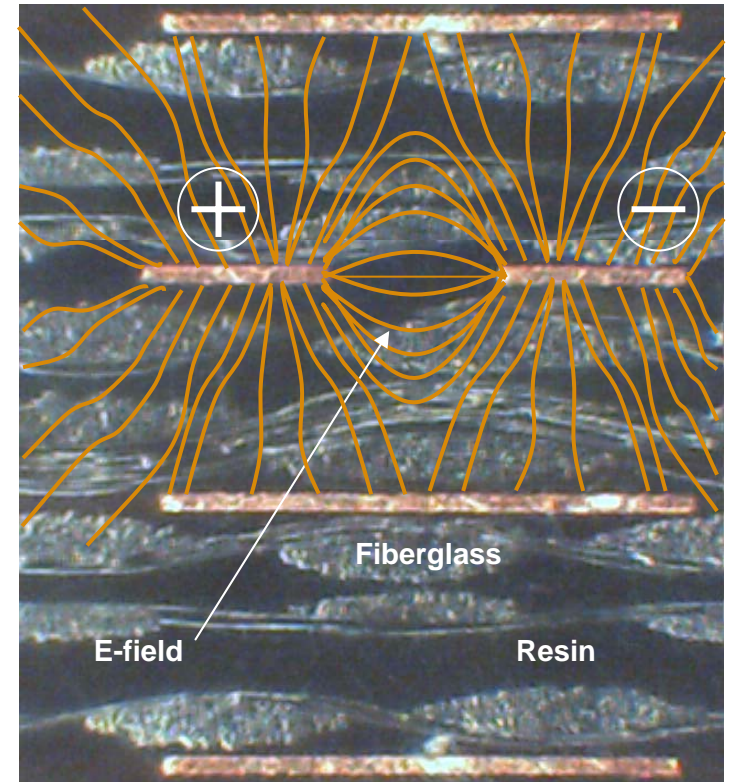
# Laminate Weave Effect

## Vias



***Higher glass to resin ratio between charges => Higher effective dielectric constant***

## Etch

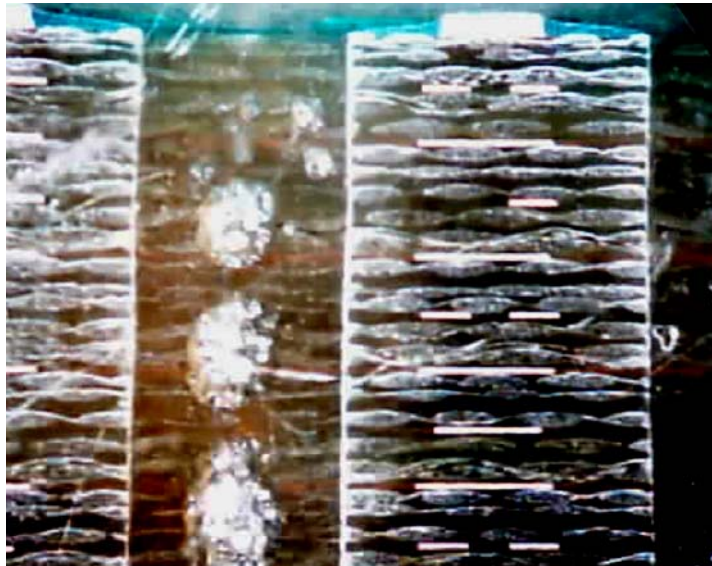
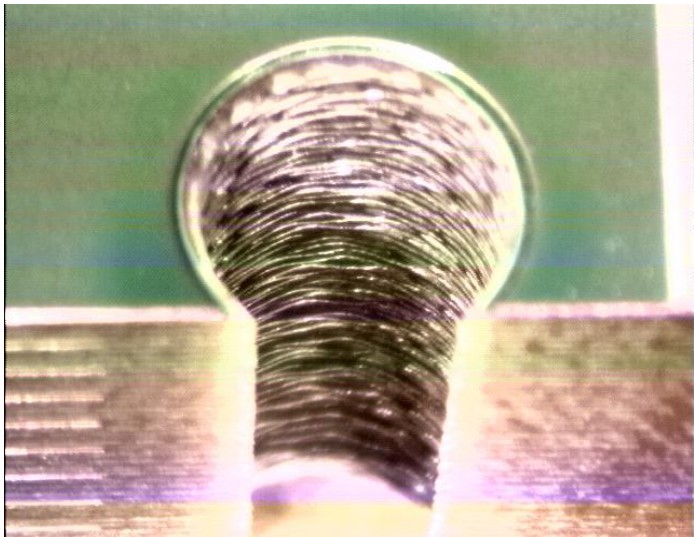
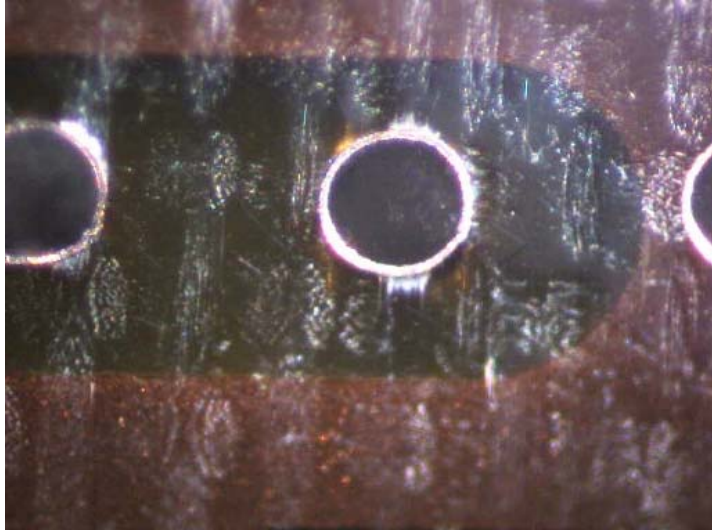
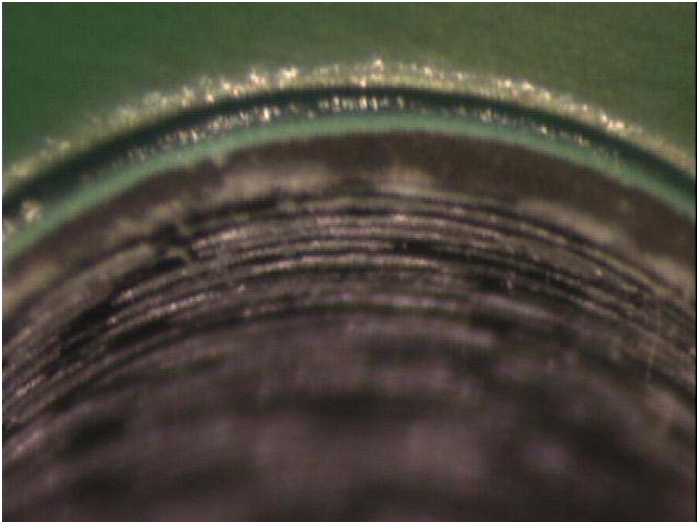


***Lower glass to resin ratio between charges => Lower effective dielectric constant***

**VS**



# Laminate Weave Effect of Via Hole Structure



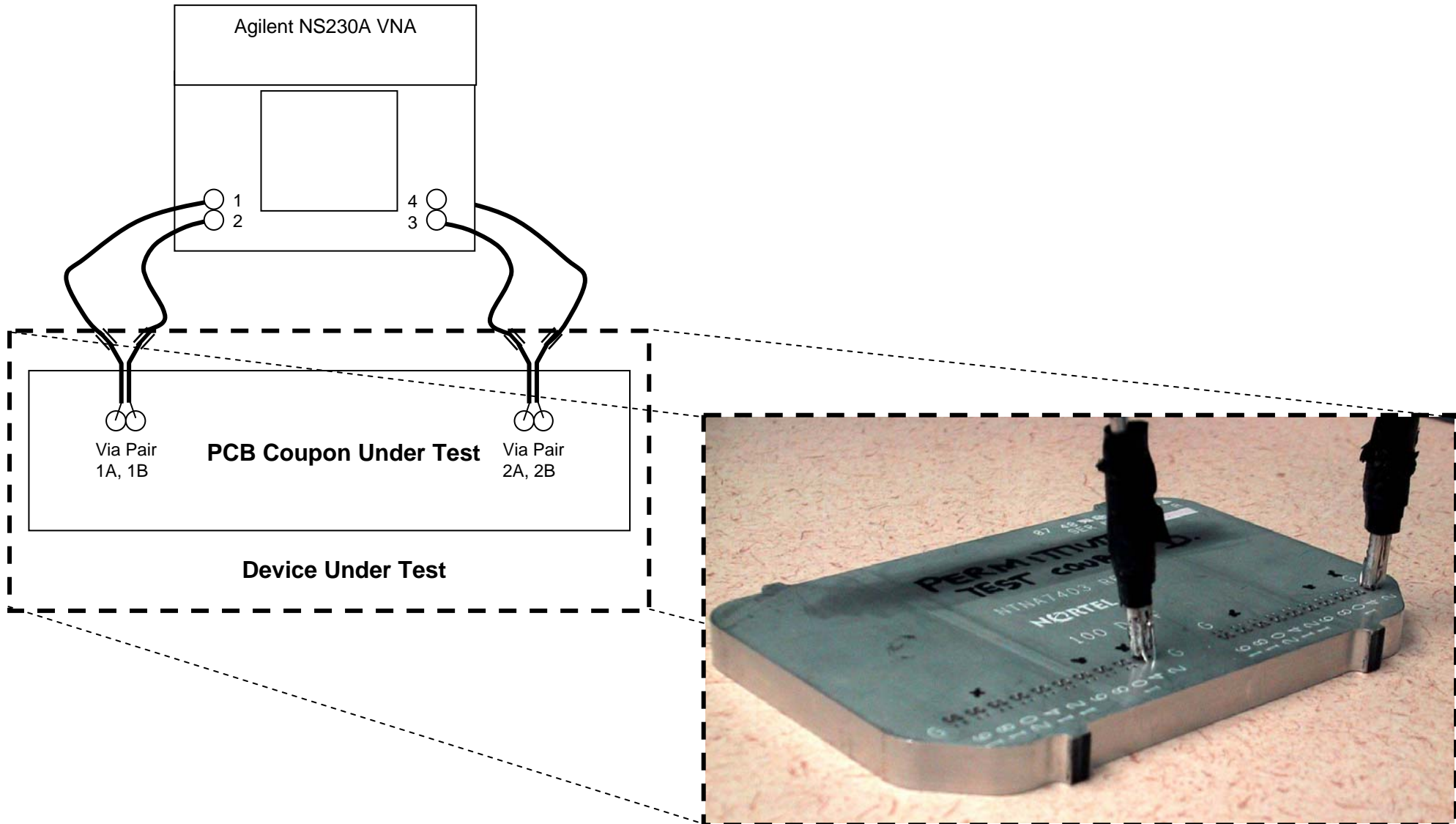
# Case Study Objective



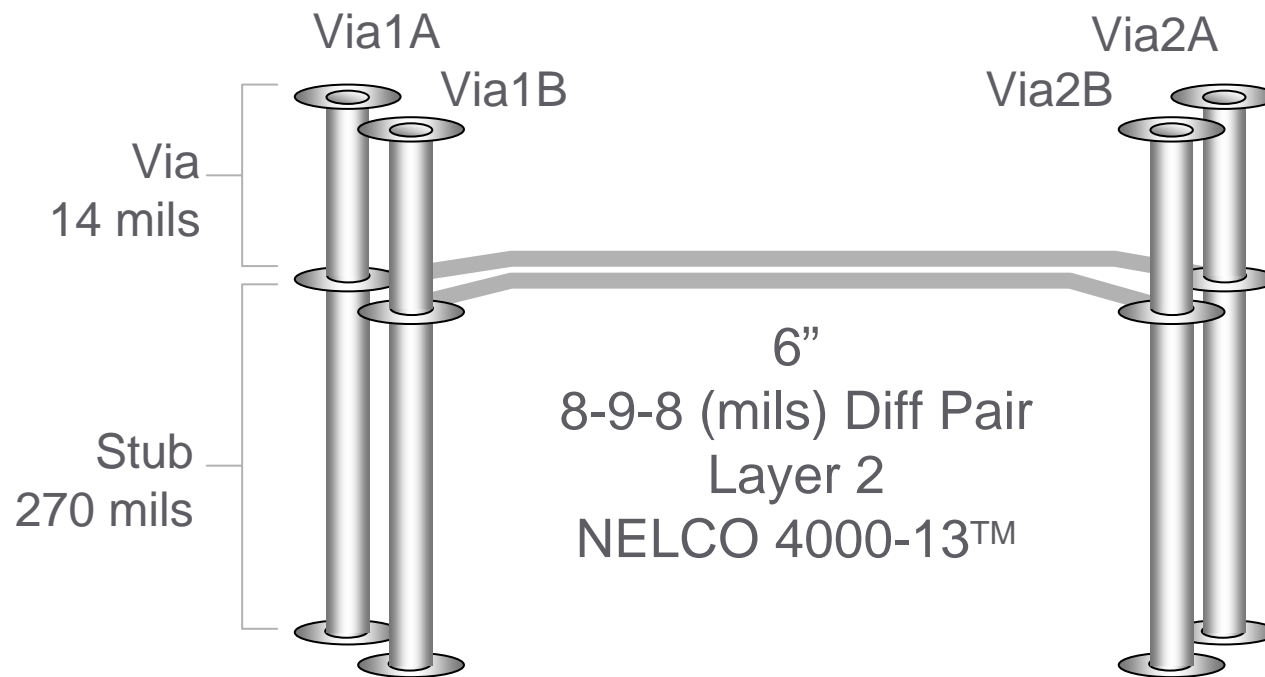
- To study the effect of relative permittivity surrounding a PCB via hole structure
- Validate transmission line via model correlation to measured results



# Test Setup

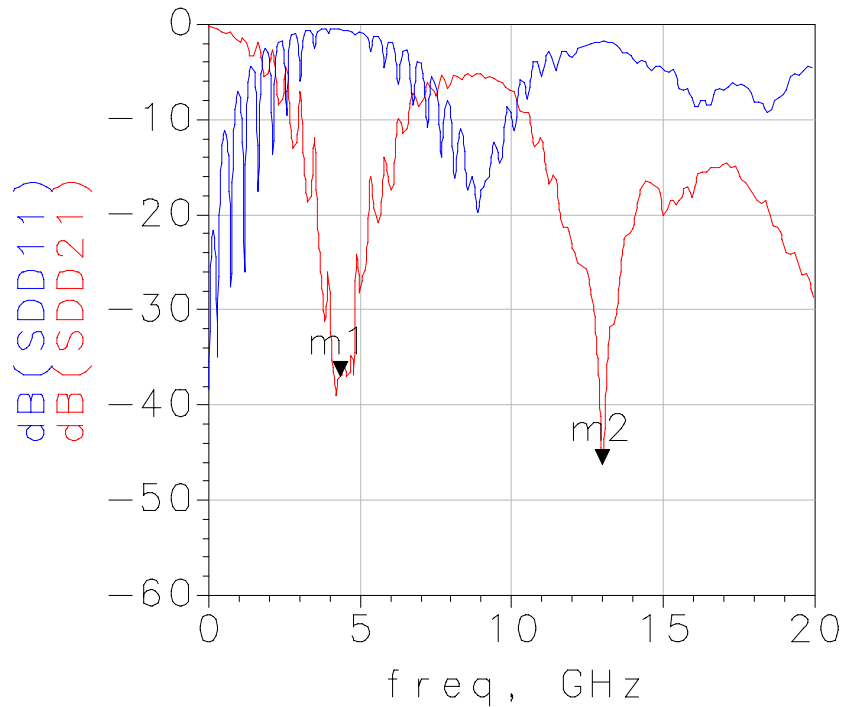


# Test Coupon Topology





# Data and Results



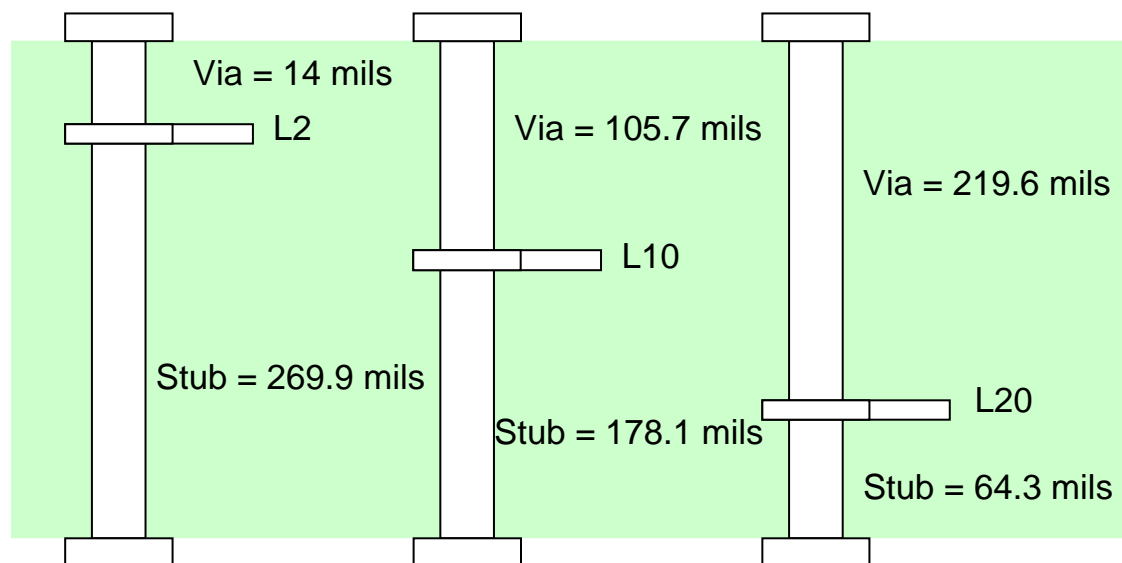
m 1
freq = 4 . 3 3 0 GHz
dB ( S D D 2 1 ) = - 3 7 . 0 0 7
m 2
freq = 1 3 . 0 0 0 GHz
dB ( S D D 2 1 ) = - 4 6 . 1 5 5

- Resonant frequency nulls due to the via stub length occur at odd harmonics of the  $\frac{1}{4}$  wave frequency null
- Effective relative permittivity (a.k.a. dielectric constant  $Dk$ ) can be calculated by [5];

$$Dk = \left[ \frac{c}{4 * Stub\_length * f} \right]^2$$
$$= 6.46$$

Where:  $c$  = Speed of light ( $1.18E10$  inches/sec);  $Stub\_Length$  (0.270) inches;  $f$  =  $\frac{1}{4}$  wave frequency (13.00GHz/3)

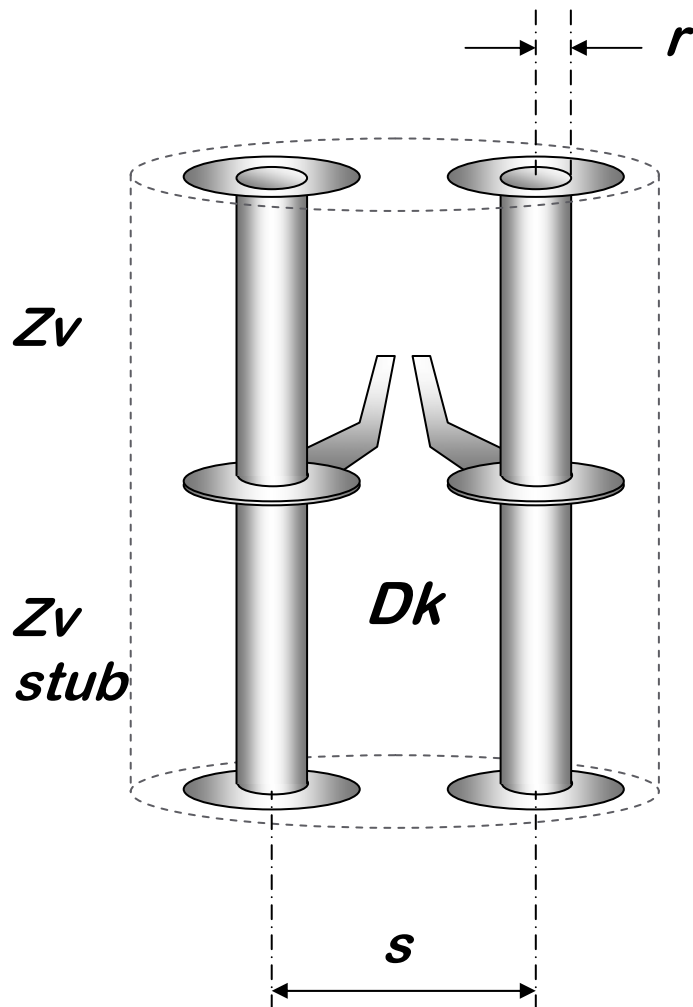
# Data and Results



Stripline Layer	$\frac{1}{4}$ Wave Frequency (GHz)	$3^{\text{rd}}$ Harmonic Frequency (GHz)	Via/Stub Lengths (Mils)	Calculated Dk
02	4.3	13.0	14/269.9	6.46
10	6.3	18.9	105.7/178.1	6.90
20	18.4	N/A	219.6/64.3	6.20



# Differential Pair Via Model



- Modeled as differential pair transmission lines
- Analogous to a twin-round-wire wire structure

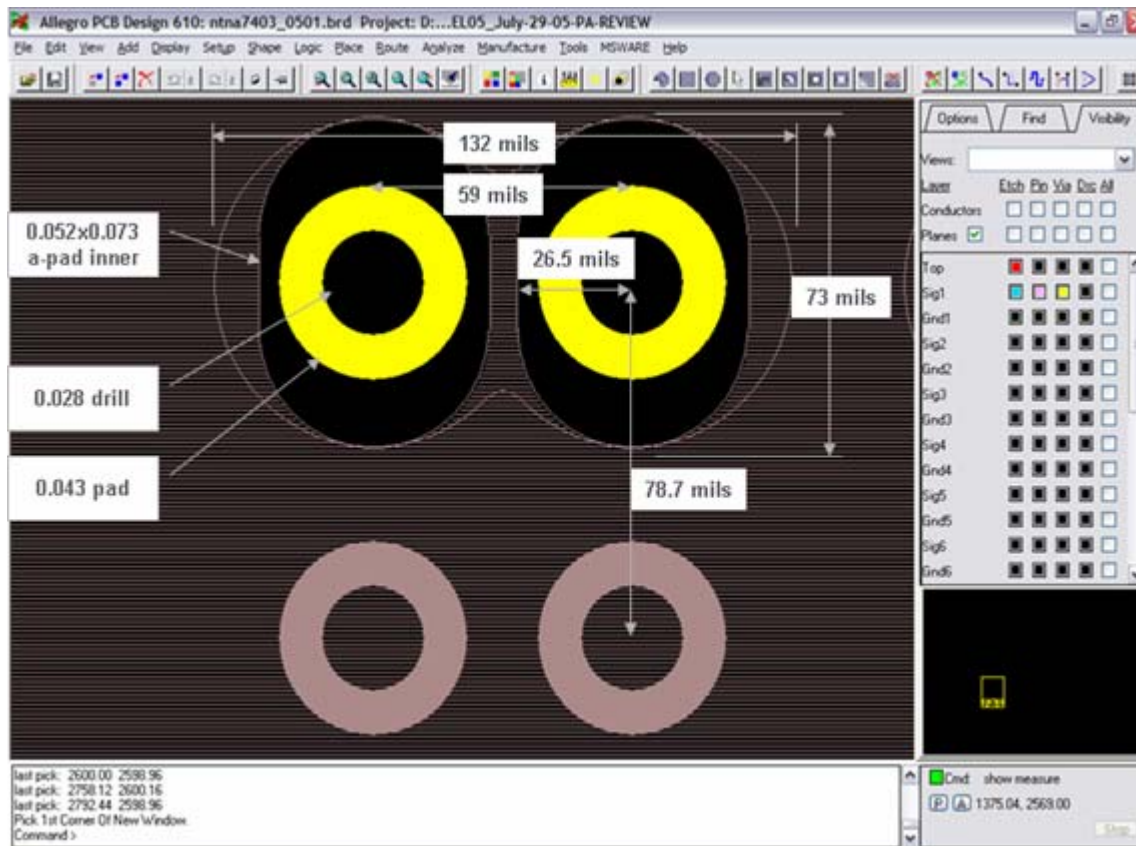
$$Z_{diff} = \frac{120\Omega}{\sqrt{Dk}} \ln \left( \frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1} \right)$$

Where:  $Z_{diff}$  = Differential impedance;  $Dk$  = Dielectric constant;  $s$  = center-to-center space of vias;  $r$  = radius of drill [6]

- Odd mode via impedance ( $Z_v$ )

$$Z_v = \frac{Z_{diff}}{2}$$

# Via Impedance Calculation



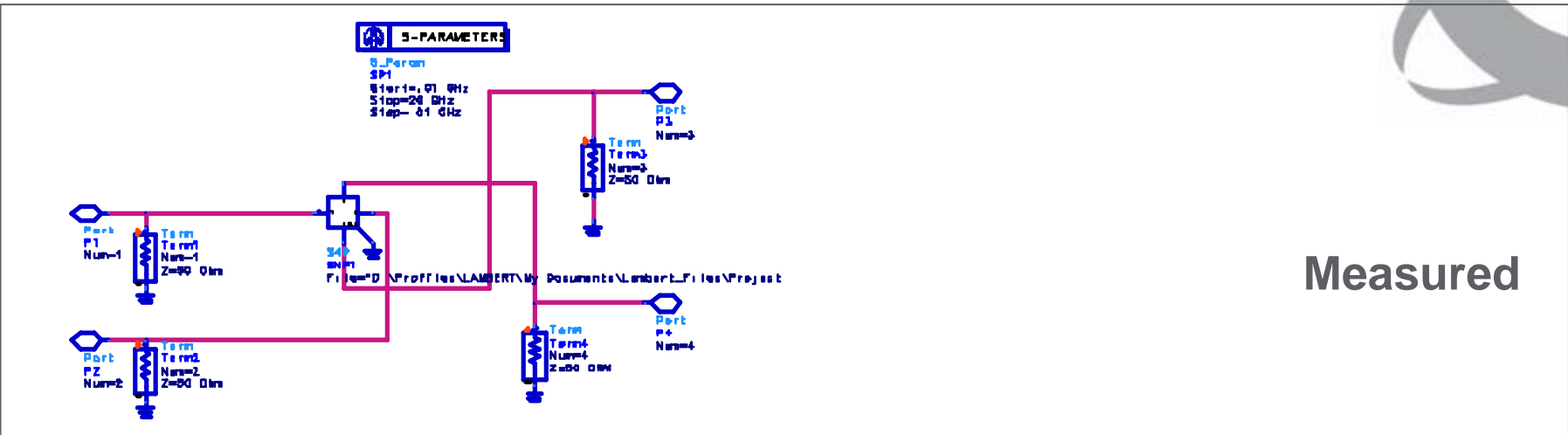
$$Z_{diff} = \frac{120\Omega}{\sqrt{Dk}} \ln \left( \frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1} \right)$$

$$= \frac{120\Omega}{\sqrt{6.4}} \ln \left( \frac{59}{28} + \sqrt{\left(\frac{59}{28}\right)^2 - 1} \right)$$

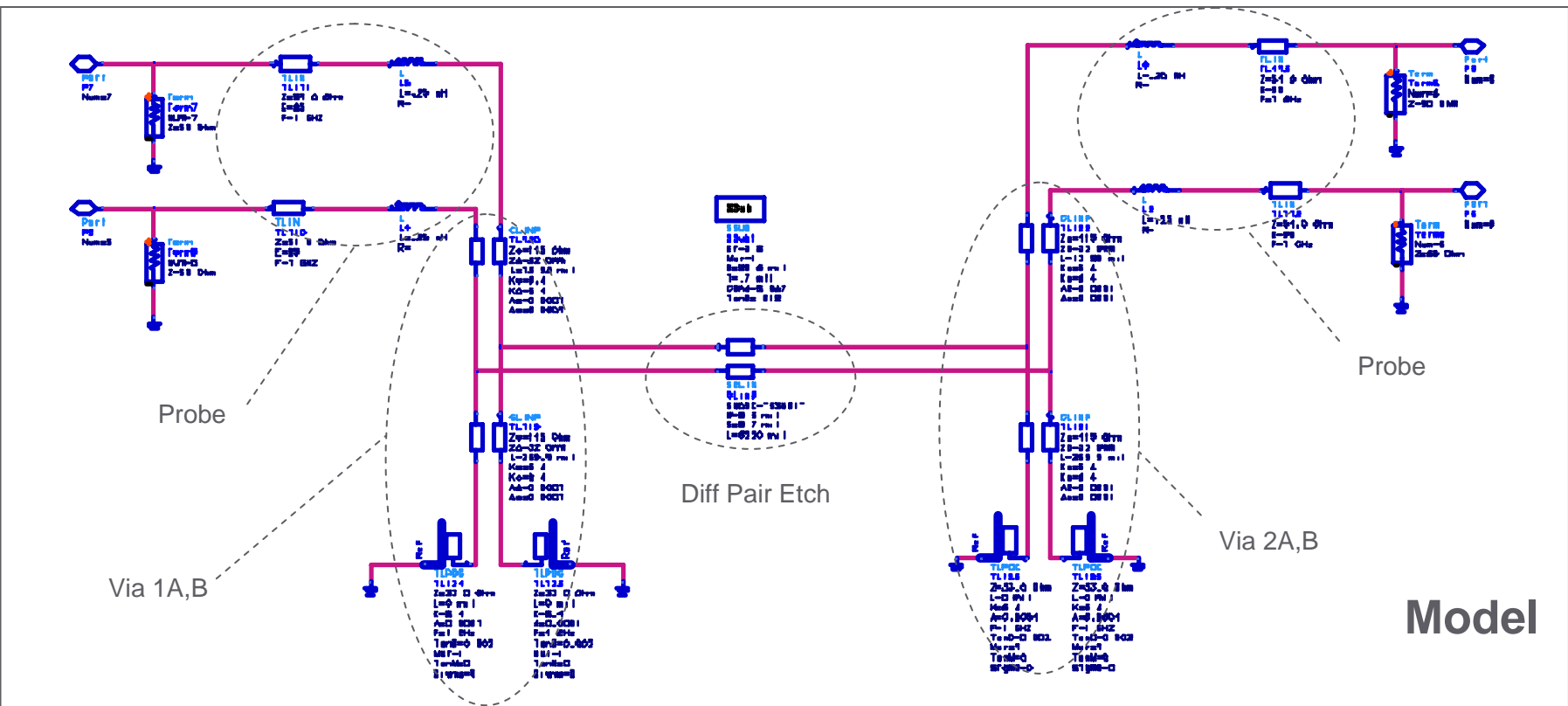
$$= 65\Omega$$

$$Z_v = Z_{odd} = \frac{Z_{diff}}{2} = \frac{65}{2} = 32.5\Omega$$

# ADS Simulation Correlation Topology



Measured



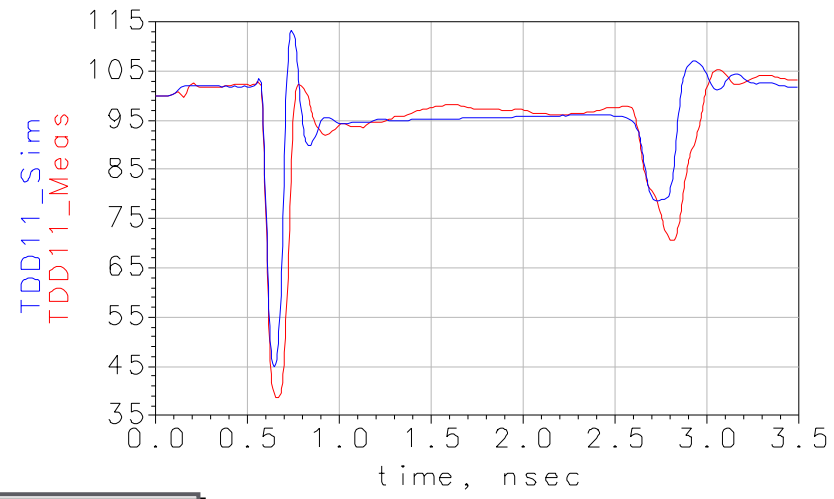
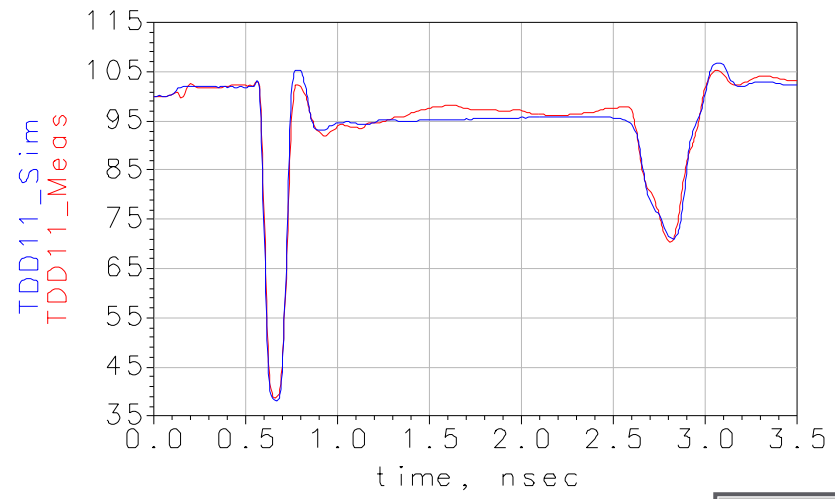
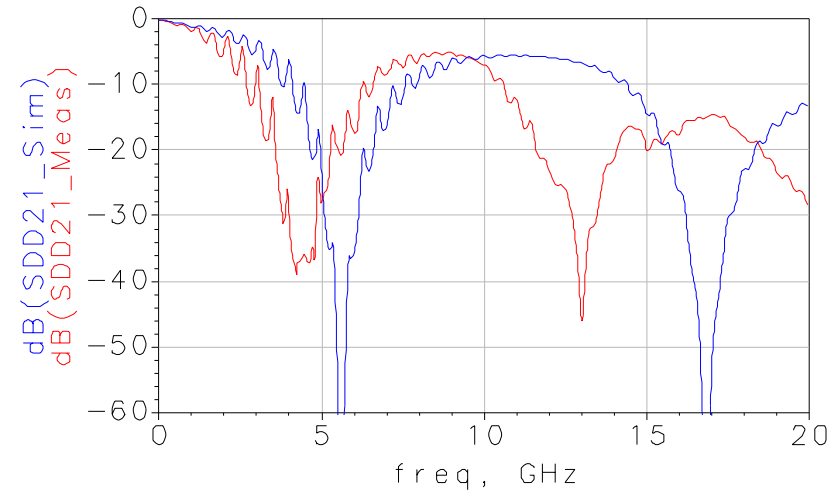
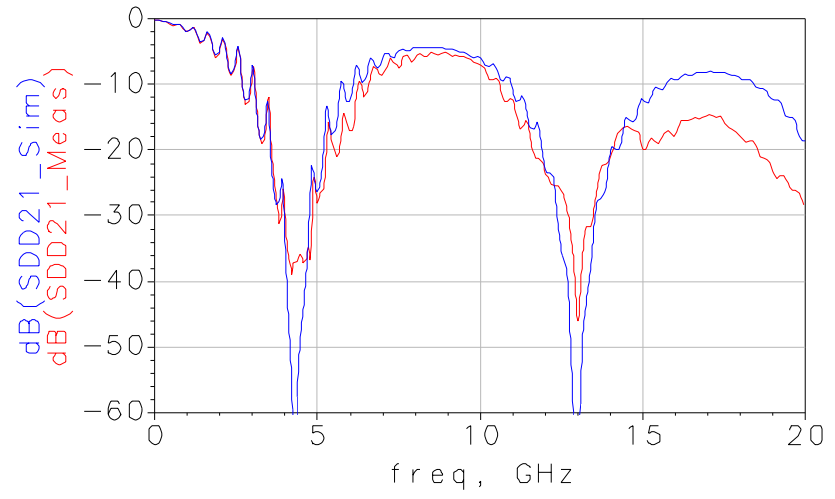
Model



# ADS Simulation Correlation Results

**Dk = 6.4**

**Dk = 3.8**



-- Measured -- Simulated





# Conclusions

- Due to the fiberglass weave effect surrounding differential pair vias, the relative permittivity is higher than the dielectric surrounding wiring etch within the same PCB stackup
- Using the correct value of dielectric constant has shown better accuracy for via modeling during topology simulations



# References

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3. Gustavo Blando, Jason R. Miller, Istvan Novak, “Losses Induced by Asymmetry in Differential Transmission Lines”, DesignCon 2007.
4. Howard Johnson, Martin Graham, “High Speed Digital Design, a Handbook of Black Magic”.
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9. Taras Kushta, Kaoru Narita, Tomoyuki Kaneko, Takanori Saeki, and Hirokazu Tohya, “Resonance Stub Effect in a Transition From a Through Via Hole to a Stripline in Multilayer PCBs”, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 13, NO. 5, MAY 2003.
10. Miroslav Pajovic, Jinghan Yu, and Dragan Milojkovic, “Analysis of Via Capacitance in Arbitrary Multilayer PCBs”, IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 49, NO. 3, AUGUST 2007.