Practical Fiber Weave Effect Modeling

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Fiber weave effect is becoming more of an issue as bit rates continue to sore upwards to 5GB/s and beyond. Due to the non-homogenous nature of printed circuit board laminates, the fiberglass weave pattern causes signals to propagate at different speeds within differential pair traces; causing timing skew and mode conversion at the receiver; leading to reduced bit-error-rate (BER) performance; and increased EMI radiation. The relative dielectric constant (Dk) surrounding a trace ultimately determines its propagation delay. This paper delves into the issue and presents a novel approach to practically establish worst case min/max values for Dk and use them to model this effect using Agilent EEofEDA circuit modeling software. A PCIe CEM Rev2 case study is used to practically demonstrate the model and to explore the design space.