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PCB Interconnect Modeling Demystified

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Abstract

In order to ensure first time success for 28GB/s and above, accurate interconnect modeling is a prerequisite. Although many EDA tools include the latest and greatest models for conductor surface roughness and wide-band dielectric properties, obtaining the right parameters to feed the models is always a challenge. So how do we get these parameters? Often the only sources are from data sheets. In most cases the numbers do not translate directly into parameters needed for these tools. By using dielectric material properties, copper foil and oxide alternative roughness parameters from data sheets, a practical method of modeling high-speed PCB interconnect is presented and correlated to measured data.

Author(s) Biography

Lambert (Bert) Simonovich graduated in 1976 from Mohawk College of Applied Arts and Technology, located in Hamilton, Ontario Canada, as an Electronic Engineering Technologist. Over a 32-year career, working at Bell Northern Research/Nortel in Ottawa, Canada, he helped pioneer several advanced technology solutions into products. He has held a variety of engineering, research and development positions; eventually specializing in high-speed signal integrity and backplane architectures. After leaving Nortel in 2009, he founded Lamsim Enterprises Inc., where he continues to provide innovative signal integrity and backplane solutions as a consultant. He has also authored and coauthored several publications. His current research interests include high-speed signal integrity, modeling and characterization of high-speed serial link architectures.

Introduction

When starting a new project board designers are often overwhelmed when trying to choose appropriate diff pair geometry, board material and stackup to meet insertion loss budgets. Part of the challenge for printed circuit board (PCB) interconnect is modeling transmission lines accurately.

At high frequencies, conductor and dielectric losses lead to dispersion of the transmitted signal. The total loss of the transmission line is the sum of dielectric and conductor losses. Predicting total loss with smooth copper and published loss tangent values is no longer adequate in the 10-plus GB/s regime.

Failure to account for conductor roughness can be problematic; especially when trying to meet the latest industry standards for 28 GB/s non-return to zero (NRZ) or 56 GB/s pulse amplitude modulation-4 level (PAM-4).

For example, the plot at the top figure of Figure 1 compares insertion loss (IL) of a differential transmission line modeled with smooth vs rough copper. For 56GB/s PAM-4 data rate, the baud rate is 28 GBd/s. With just 3.4 dB delta in IL at 14 GHz Nyquist frequency, results in a reduction of 17% in eye height and 1% increased jitter, averaged across all three eyes.

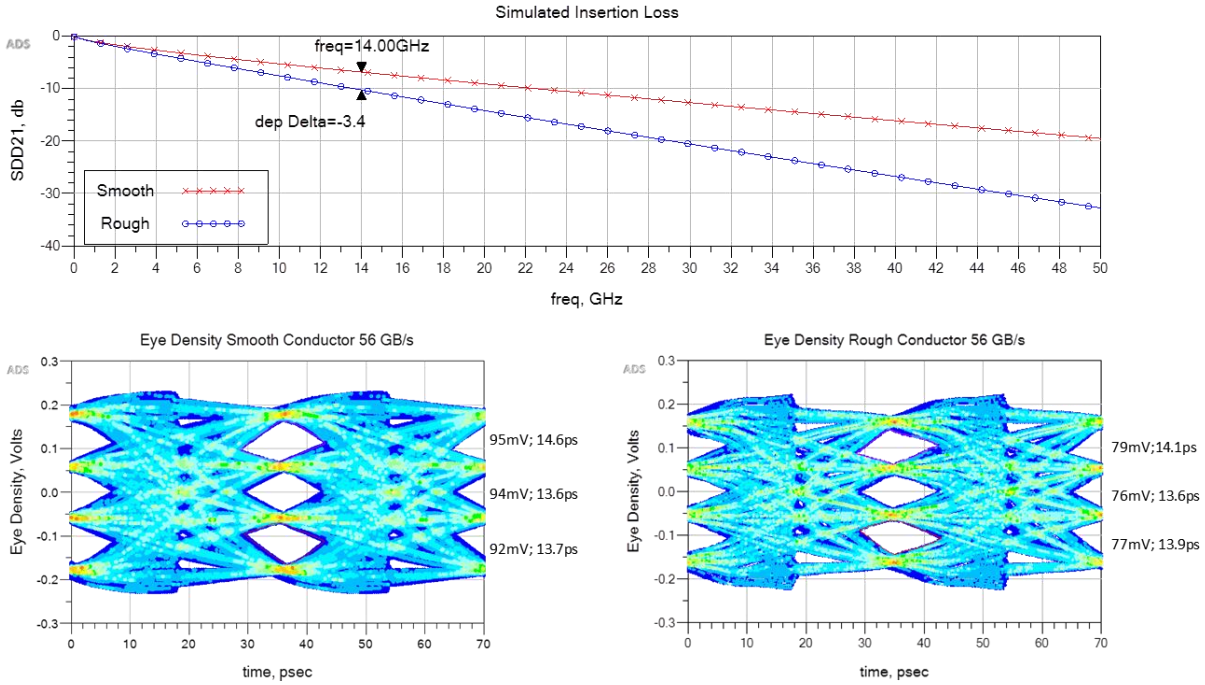


Figure 1 Simulated results of a differential transmission line modeled with and without conductor roughness taken into account.

Furthermore, as we will see later, failure to correct dielectric constant (D_k) from manufacturers' data sheets due to conductor roughness can lead to inaccuracy in phase delay [1].

Many electronic design automation (EDA) tools include the latest and greatest models for conductor surface roughness and wide-band dielectric properties. But obtaining the right parameters to feed the models is always a challenge for designers.

There are those who advocate using the design feedback method to get these parameters. This involves designing, building and measuring a test coupon. After modeling and tuning various parameters to best fit measured data, material parameters are extracted and used in channel modeling software to design the final product.

The problem with this approach for many small companies is: TIME, RESOURCES, and MONEY.

- Time to define stackup and test structures.
- Time to actually design a test coupon.
- Time to procure raw material - can take weeks, depending on scarcity of core/prepreg material.
- Time to fabricate the bare PCB.
- Time to assemble and measure.
- Time to cross-section and measure parameters.
- Time to model and fit parameters to measurements.

Then there is the issue of resources, which include the right test equipment and trained personnel to get trusted measurements.

In the end this process ultimately costs more money, and material properties are only accurate for the sample from which they were extracted for the software and roughness model used. There is no guarantee extracted parameters to feed the respective models reflect the true material properties.

But, as Eric Bogatin often likes to say [24], *"Sometimes an OK answer NOW is better than a good answer late"*. For many signal integrity engineers, they have to come up with an answer sooner, rather than later, because of time to market challenges.

So where do we get these parameters? Often the only sources are from manufacturers' data sheets alone. But in most cases, the numbers do not translate directly into parameters needed for the EDA tools.

In this paper you will learn:

- How to determine effective dielectric constant (D_{keff}) due to roughness from data sheets alone.
- How to apply a simple Cannonball stack model [2] to determine roughness parameters needed for Huray model [4] from data sheets alone.
- How to apply these parameters in popular field solvers.
- Impact of causal metal model to simulated results.
- Impact of Oxide/Oxide Alternative treatments on roughness, insertion loss and impedance.

- How to pull it all together and compare simulated transmission line interconnect models with case studies; including a practical backplane channel model example.

Background

Electro-deposited Copper

There are two types of copper foil used in PCB industry. Rolled-annealed (RA) and electro-deposited (ED) copper. RA copper is smoother than ED copper, but ED copper is widely used in the PCB industry due to its low cost.

A finished sheet of ED foil has a matte side and drum side. The matte side is usually treated with tiny nodules and is the side bonded to the core laminate. The drum side is always smoother than the matte side. For high frequency boards, sometimes the drum side of the foil is treated instead and bonded to the core. In this case it is known as reversed treated foil (RTF).

Profilometers are often used to quantify the roughness tooth profile of electro-deposited copper. Nodule treated tooth profiles are typically reported in terms of 10-point mean roughness (R_z). For standard foil this is the matte side. For RTF it is the drum side. Most often the untreated, or prepreg side, reports average roughness (R_a) in manufacturers' data sheets. Some manufacturers may also report root mean square (RMS) roughness (R_q).

Various foil manufacturers offer ED copper foils with varying degrees of roughness. Each supplier tends to market their product with their own brand name. Presently, there are three distinct classes of copper foil roughness:

- Standard
- Very-low profile (VLP)
- Ultra-low profile (ULP) or profile-free (PF)

Standard ED foils have no maximum spec. With the realization of roughness having a detrimental effect on insertion loss (IL), copper suppliers began providing VLP and ULP foils. VLP foils have treated roughness profiles less than 4 μm while ULP foils are less than 2 μm. Some other common names referring to ULP class are HVLP or eVLP.

Oxide/Oxide Alternative Treatment

In order to promote good adhesion of copper to the prepreg material during the PCB lamination process, the copper surface is treated with chemicals to form a thin, nonconductive film of black or brown oxide. The controlled oxidation process increases the surface area, which provides a better bond between the prepreg and the copper surface. It also passivates the copper surface to protect it from contamination.

Oxide treatment has been used for many years. But eventually the industry learned that the lack of chemical resistance, during the PCB fabrication process, resulted in pink ring. Pink ring is the region around a hole that looks pink where the oxide has dissolved due to cleaning and plating chemicals attacking the oxide layer. It is indicative of poor adhesion between copper and prepreg.

The inherent oxide weakness has led to oxide alternative (OA) treatments during the late 1990s. They still rely on some sort of etching process, but no oxide layer is formed.

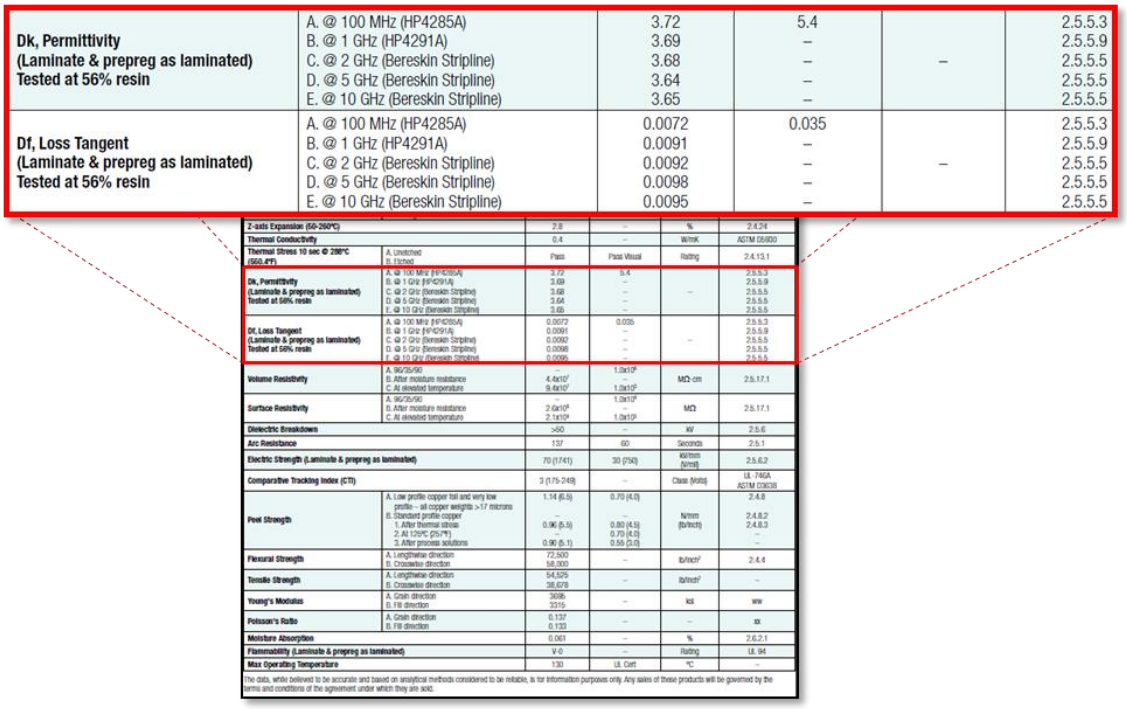
With the push for smoother copper to reduce conductor loss, newer chemical bond enhancement treatments, working at the molecular level, were developed to maintain copper smoothness, yet still provide good bonding to the prepreg.

Later we will see the impact of OA treatment on insertion loss and impedance.

Effective D_k Due to Roughness

Everyone involved in the design and manufacture of PCBs knows the most important properties of the dielectric material are the dielectric constant (D_k) and dissipation factor (D_f).

Using D_k / D_f numbers for stackup design and channel modeling from "Marketing" data sheets, like the example shown in Figure 2 [10], will give inaccurate results. These data sheets are easily obtained when searching laminate supplier's web sites.



Dk, Permittivity (Laminate & prepreg as laminated) Tested at 56% resin	A. @ 100 MHz (HP4285A)	3.72	5.4		2.5.5.3
	B. @ 1 GHz (HP4291A)	3.69	–		2.5.5.9
	C. @ 2 GHz (Bereskin Stripline)	3.68	–	–	2.5.5.5
	D. @ 5 GHz (Bereskin Stripline)	3.64	–		2.5.5.5
	E. @ 10 GHz (Bereskin Stripline)	3.65	–		2.5.5.5
Df, Loss Tangent (Laminate & prepreg as laminated) Tested at 56% resin	A. @ 100 MHz (HP4285A)	0.0072	0.035		2.5.5.3
	B. @ 1 GHz (HP4291A)	0.0091	–		2.5.5.9
	C. @ 2 GHz (Bereskin Stripline)	0.0092	–	–	2.5.5.5
	D. @ 5 GHz (Bereskin Stripline)	0.0098	–		2.5.5.5
	E. @ 10 GHz (Bereskin Stripline)	0.0095	–		2.5.5.5

Figure 2 Example of a "Marketing" data sheet easily obtained from laminate supplier's web site [10].

Instead, real or "Engineering" data sheets, which are used by PCB fabricators to design stackups, should be used for interconnect modeling. An example is shown in Figure 3 [10]. These data sheets define the actual thickness, resin content and glass style for different cores and prepregs. They include D_k / D_f over a wide frequency range; usually from 100 MHz-10GHz.

Many engineers assume D_k published is the intrinsic property of the material. But in actual fact, it is the effective dielectric constant (D_{keff}) generated by a specific test method. When simulations are compared against measurements, there is often a discrepancy in D_{keff}, due to increased phase delay caused by surface roughness.

Core Data

Core Constructions	Resin Content (%)	Thickness (inch)	Thickness (mm)	Dielectric Constant(DK) / Dissipation Factor(DF)							
				100 MHz	500 MHz	1.0 GHz	2.0 GHz	5.0 GHz	10.0 GHz	15.0 GHz	20.0 GHz
1x106	72.0	0.0020 ZBC	0.0508 ZBC	3.37	3.36	3.34	3.32	3.30	3.30		
				0.0075	0.0089	0.0096	0.0101	0.0107	0.0107		
1x1067	69.0	0.0025	0.0635	3.42	3.40	3.38	3.36	3.34	3.33		
				0.0075	0.0084	0.0095	0.0100	0.0105	0.0104		
1x1080	57.0	0.0025	0.0635	3.67	3.64	3.62	3.61	3.60	3.59		
				0.0071	0.0079	0.0089	0.0092	0.0097	0.0095		
1x1086	58.0	0.0030	0.0762	3.65	3.63	3.60	3.59	3.57	3.57		
				0.0072	0.0079	0.0091	0.0092	0.0098	0.0095		
1x1080	63.0	0.0030	0.0762	3.54	3.52	3.50	3.48	3.47	3.47		
				0.0074	0.0082	0.0092	0.0096	0.0102	0.0101		
1x3313	51.0	0.0035	0.0889	3.82	3.79	3.77	3.77	3.74	3.74		
				0.0068	0.0076	0.0084	0.0087	0.0092	0.0090		
2x106	67.0	0.0035	0.0889	3.46	3.45	3.42	3.40	3.38	3.37		
				0.0074	0.0083	0.0094	0.0098	0.0104	0.0102		
106/1080	59.0	0.0040	0.1016	3.63	3.61	3.58	3.57	3.55	3.54		
				0.0072	0.0080	0.0090	0.0093	0.0098	0.0096		
1x3313	55.0	0.0040	0.1016	3.72	3.70	3.68	3.66	3.65	3.65		
				0.0071	0.0077	0.0087	0.0090	0.0095	0.0094		
106/1080	61.0	0.0043	0.1092	3.57	3.56	3.54	3.52	3.51	3.50		
				0.0073	0.0081	0.0092	0.0095	0.0099	0.0098		
2x1067	63.0	0.0043	0.1092	3.54	3.52	3.50	3.48	3.47	3.47		
				0.0074	0.0082	0.0092	0.0096	0.0102	0.0101		
106/1080	62.0	0.0045	0.1143	3.55	3.54	3.52	3.50	3.48	3.48		
				0.0073	0.0082	0.0092	0.0095	0.0100	0.0098		

Figure 3 Example of an "Engineering" data sheet used by PCB fabricators to design stackup [10].

D_{keff} is highly dependent on the test apparatus and conditions of how it is measured. One method commonly used by many laminate suppliers is the clamped stripline resonator test method, as described by IPC-TM-650 Test Methods Manual [14]. Section 2.5.5.5 Rev C defines test methods to rapidly test dielectric material for permittivity and loss tangent over an X-band frequency range of 8-12.4 GHz in a production environment.

The measurements are done under stripline conditions using a carefully designed resonant element pattern card made with the same dielectric material to be tested. The card is sandwiched between two sheets of unclad dielectric material under test. The whole structure is then clamped between two large plates; each lined with copper foil and are grounded. They act as reference planes for the stripline.

By measuring the resonant frequency of the cavity, D_k and D_f are determined. This method assures consistency of product when used in fabricated boards. It does not guarantee the values directly correspond to design applications.

This is a key point to keep in mind, and here is why.

Since the resonant element pattern card and material under test are not physically bonded together, as it would be the case in real life, there are small air gaps between the various layers that affect measured results. They are caused, in part, by removing the copper from material under test, thereby leaving the microvoid imprint for the copper roughness on the bare substrate surface. The air gaps result in a lower D_{keff} than what is measured in real applications using foil with different roughness bonded to the same core laminate. This is the primary reason for phase delay discrepancy between simulation and measurements.

In my DesignCon 2017 paper [1] I showed that if D_k and R_z roughness parameters from the manufacturers' data sheets are known, then the effective D_k due to roughness (D_{keff_rough}) of the fabricated core laminate can be easily estimated by:

Equation 1

$$D_{keff\_rough} \approx \frac{H_{smooth}}{\left(H_{smooth} - 2R_z\right)} \times D_k$$

where:

H_{smooth} is the thickness of dielectric from data sheet

R_z is 10-point mean roughness from data sheet

D_k is dielectric constant from data sheet

Causal Dielectric models

Referring to the data sheet in Figure 3 we see that D_k and D_f varies over frequency. If the complex dielectric constant ε is defined as:

Equation 2

$$\varepsilon = \varepsilon' - j\varepsilon''$$

then:

Equation 3

$$\tan(\delta) = \frac{\varepsilon''}{\varepsilon'}$$

If the real part $\varepsilon' = D_k$ and $\tan(\delta) = D_f$, then:

Equation 4

$$D_f = \frac{\varepsilon''}{D_k}$$

If we know the real part, D_k from the data sheet, then the imaginary part ε'' is also known through the Kramers-Kronig relations, which links the relationship between the real and imaginary parts of any complex function [15].

Because of this, we need to use a causal dielectric model which ensures that an effect cannot happen before its cause. Most EDA tools include a wideband causal model. To use it, you must enter D_k and D_f at a particular frequency. I found it is usually best to use the values near the Nyquist frequency of the baud rate.

Skin Effect

Alternating current (AC) causes conductor loss to increase in proportion to the square root of frequency. This is due to the redistribution of current towards the outer edges caused by skin-effect. The resulting skin-depth (δ) is the effective thickness where the current flows around the perimeter and is a function of frequency.

Skin-depth at a particular frequency is determined by:

Equation 5

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma}}$$

where:

δ = skin-depth in meters

f = sine-wave frequency in Hz

μ_0= permeability of free space =1.256E-6 Wb/A-m

σ = conductivity in S/m. For annealed copper σ = 5.80E7 S/m

At high frequencies, when the skin depth approaches the height of the roughness profile of the copper, it starts to affect the electromagnetic properties of the transmitted signal.

Modeling Copper Roughness

"All models are wrong but some are useful"- a famous quote by George E. P. Box, who was a British statistician in the mid-20th century. The same can be said when using various roughness models.

For example many roughness models require RMS roughness numbers, but often R_z is the only number available in data sheets, and vice versa. If R_z is defined as the sum of the average of the five highest peaks and the five lowest valleys of the roughness profile over a sample length, then the roughness can be modeled as a triangular profile with a peak to valley height equal to R_z, as illustrated in Figure 4.

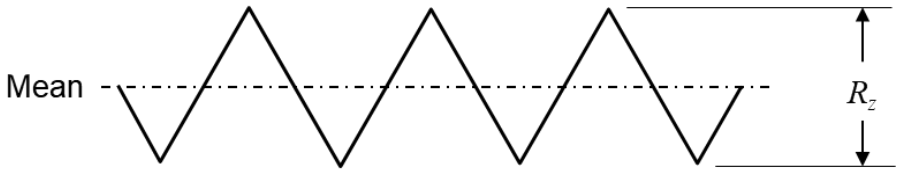


Figure 4 Triangular roughness profile model with peak to valley height equal to 10-point mean roughness R_z.

If we define the RMS height of the triangular roughness profile is equal to Δ, then:

Equation 6

$$\Delta = \frac{R_z}{2\sqrt{3}}$$

And likewise, if we assume $\Delta \approx R_q$, then:

Equation 7

$$R_z \approx R_q\left(2\sqrt{3}\right)$$

Several modeling methods were developed over the years to determine a roughness correction factor (K_{SR}). When multiplicatively applied to the smooth conductor attenuation (α_{smooth}), the attenuation due to roughness (α_{rough}) can be determined by:

Equation 8

$$\alpha_{rough} = K_{SR}\alpha_{smooth}$$

Hammerstad & Jensen Model

The Hammerstad & Jensen (H&J) model [3] assumes a triangular corrugated surface representing the tooth structure of rough copper, as shown in Figure 5. For many years people believed that when the skin depth is small, compared to the tooth height, current flows along the corrugated surface, thereby increasing its loss due to the longer path length. And for many years this was a useful explanation.

However, this theory breaks down from a physics perspective because there is no evidence of additional time delay (*TD*), compared to the fixed spatial length of the trace. Any perceived increase in time delay than expected is explained by the higher D_{keff} due to roughness [1] and increased internal inductance of the rough metal [21], as we will see later.

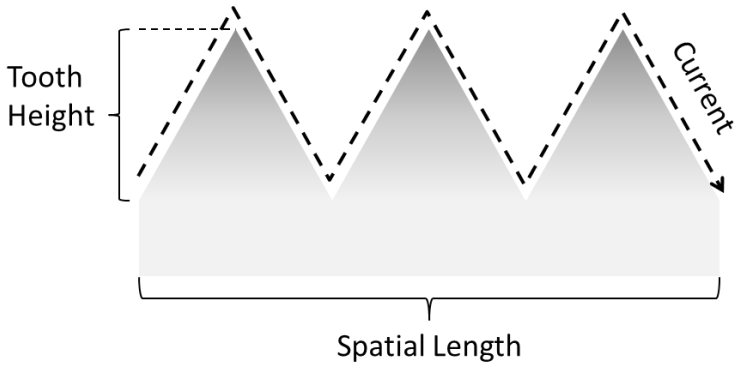


Figure 5 A two-dimensional surface profiles the H&J model is based on.

The H&J correction factor (K_{HJ}), at a particular frequency, is determined by:

Equation 9

$$K_{HJ} = 1 + \frac{2}{\pi}\arctan\left(1.4\left(\frac{\Delta}{\delta}\right)^2\right)$$

where:

K_{HJ} = H&J roughness correction factor

Δ = RMS height of the peak to valley tooth height in meters

δ = skin depth in meters

Figure 6 shows simulated results of a another example of a model being wrong but still useful up to 12GHz before it starts to lose accuracy supporting Box's famous quote!

Figure 6 Plot showing H&J model accuracy compared to measured data. In this case the model is only good to 12GHz before losing accuracy.

Huray Model

In recent years, the Huray model [4] has gained popularity due to the continually increasing data rate's need for better modeling accuracy. The model is based on a non-uniform distribution of spherical shapes resembling "snowballs" and stacked together forming a pyramidal geometry.

By applying electromagnetic wave analysis, the superposition of the sphere losses can be used to determine the total loss of the structure. Since the losses are proportional to the surface area of the roughness profile, an accurate estimation of a roughness correction factor (K_{SRH}) can be analytically solved by:

Equation 10

$$K_{SRH}(f) = \frac{A_{matte}}{A_{flat}} + \frac{3}{2}\sum_{i=1}^{j}\left(\frac{N_i \times 4\pi a_i^2}{A_{flat}}\right) \div \left(1 + \frac{\delta(f)}{a_i} + \frac{\delta^2(f)}{2a_i^2}\right)$$

where:

$K_{SRH}(f)$ = roughness correction factor, as a function of frequency, due to surface roughness based on the Huray model

$\frac{A_{matte}}{A_{flat}}$ = relative area of the matte base compared to a flat surface

a_i = radius of the copper sphere (snowball) of the i^{th} size, in meters

$\frac{N_i}{A_{flat}}$ = number of copper spheres of the i^{th} size per unit flat area in sq. meters

$\delta(f)$ = skin-depth, as a function of frequency, in meters

Although it has been proven to be a pretty accurate model, it relied on analysis of scanning electron microscopy (SEM) pictures of the treated surface and tuning of

parameters for best fit to measured data. This is not a practical solution if all you have is roughness parameters from manufacturers' data sheets.

Cannonball-Huray Model

Building upon the work already done by Huray, and using the Cannonball stack principle, the sphere radius and flat base area parameters are easily estimated solely from roughness parameters published in manufacturers' data sheets [2].

As illustrated in Figure 7 there are three rows of equal sized spheres stacked on a square tile base. Nine spheres are on the first row, four spheres in the middle row, and one sphere on top.

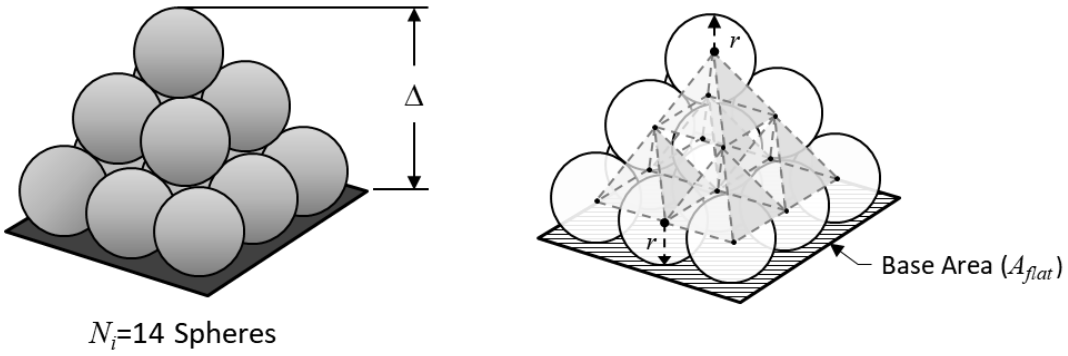


Figure 7 Cannonball-Huray physical model.

If we could peer into the stack and imagine a pyramid lattice structure connecting to the center of all the spheres, then the total height is equal the height of two pyramids plus the diameter of one sphere.

Given the height of the Cannonball stack (Δ) is equal to the RMS value of the peak to valley roughness profile; then from method described in [2], determining the sphere radius (r), from R_z found in data sheets, can be further simplified and approximated as:

Equation 11

$$r \approx 0.06 R_z$$

and base area (A_{flat}) as:

Equation 12

$$A_{flat} = 36(r)^2$$

Because the model assumes the ratio of $A_{matte}/A_{flat} = 1$, and there are only 14 spheres, the original Cannonball-Huray model can be further simplified to:

Equation 13

$$K_{CH}(f) = 1 + 2.33\pi\left(1 + \frac{\delta(f)}{r} + \frac{\delta^2(f)}{2r^2}\right)^{-1}$$

where:

K_{CH} (f) = Cannonball-Huray roughness correction factor, as a function of frequency

δ (f) = skin-depth, as a function of frequency in meters

r = the radius of spheres in meters (Equation 11)

Cannonball-Huray Model for Popular EDA Tools

Several popular EDA tools ask for input parameters for the Huray model that are not easily apparent unless you go searching in their help manual.

Ansys [25] and Cadence [26] tools require surface ratio (sr) and nodule radius (r) as input parameters. In this context, surface ratio is defined as surface area of spheres divided by the base area. Nodule radius is calculated from Equation 11.

Because the Cannonball model always has $N=14$ spheres and base area (A_{flat}) is always $36r^2$, r^2 cancels out and sr can be simplified to:

Equation 14

$$sr = \left(\frac{14 \times 4\pi r^2}{A_{flat}} \right) = \left(\frac{14 \times 4\pi r^2}{36r^2} \right) = \left(\frac{14 \times 4\pi}{36} \right) = 1.56\pi \approx 4.9$$

Mentor Hyperlynx [19]and Polar Instruments Si9000e [5] include the Cannonball-Huray model as an option, so all that needs to be entered is R_z for drum and matte side of the foil directly.

Simbeor electromagnetic signal integrity software tool, from Simberian Inc. [22], requires two parameters; roughness factor (*RF1*) and sphere radius (*SR1)*. Both are described in context later in the following case study.

Megtron-4 RTF Case Study

To test the accuracy of the model, measured data from a test platform, courtesy of Ciena Corporation [18] shown in Figure 8, was used for model validation. The 5 inch de-embedded S-parameter data was computed from a 1 inch and 6 inch differential stripline traces.

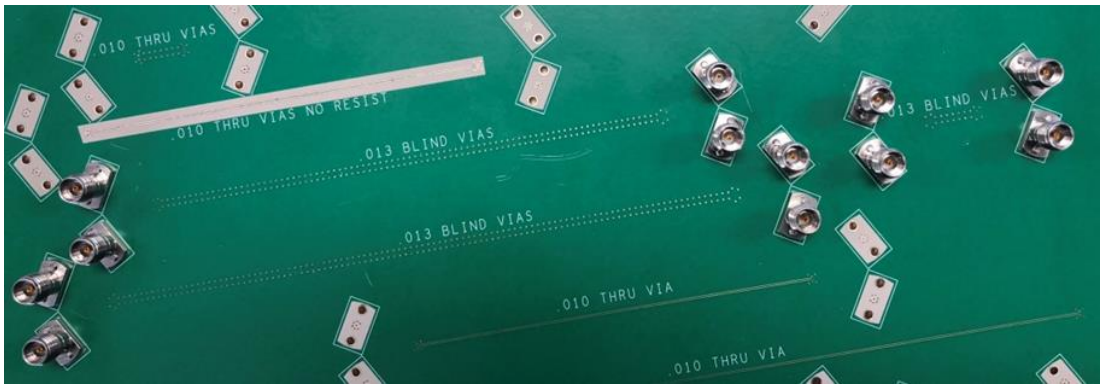


Figure 8 Photo of a portion of a Meg-4 RTF test platform courtesy of Ciena Corporation [18] used for model validation.

The PCB was fabricated with Panasonic Megtron-4 (Meg-4) [7] 1067 core and prepreg, with 0.5 oz. RTF. Table 3 summarizes the PCB design parameters, dielectric material properties and copper roughness parameters obtained from manufactures' data sheets.

An oxide or oxide alternative (OA) treatment is usually applied to the copper surfaces prior to final PCB lamination. When it is applied to the matte side of RTF, it tends to smoothen the macro-roughness slightly. At the same time, it creates a surface full of microvoids which follows the underlying rough profile and allows the resin to fill in the cavities, providing a good anchor. Typically 50 μin (1.27 μm) of copper is removed by OA treatment [12], thereby reducing the roughness to 2.13 μm.

Table 1 Meg-4 Test Board and Data Sheet Parameters

Parameter	Value
D_k Core/Prepreg @ 10GHz	3.55/3.41
D_f Core/Prepreg @ 10GHz	0.008/0.008
R_z Drum side	2.5 μm
R_z Before Micro-etch-Matte side	3.4μm
R_z After 50 μin (1.27 μm) Micro-etch treatment -Matte side	2.13 μm
Trace Thickness, *t*	0.63 mils (31.73 μm)
Trace Width Base (W1)	3.5 mils (88.9 μm)
Trace Width Top (W2)	3 mils (76.2 μm)
Space (s)	4.5 mils (114.3 μm)
Core thickness, H1	3.9 mils (99.06 μm)
Prepreg thickness, H2	3.95 mils (100.33 μm)
De-embedded trace length	5.00 in (15.24 cm)

From Table 1 and by applying Equation 1, D_{keff} of core and prepreg due to roughness were determined to be:

$$D_{keff\_Core} = \frac{H_1}{\left(H_1 - 2R_z\right)} D_{k1} = \frac{99.06\mu m}{\left(99.06\mu m - 2\left(2.5\mu m\right)\right)} \times 3.55 = 3.74$$

$$D_{keff\_prepreg} = \frac{H_2}{\left(H_2 - 2R_z\right)} D_{k2} = \frac{100.33\mu m}{\left(100.33\mu m - 2\left(2.13\mu m\right)\right)} \times 3.41 = 3.56$$

Next, the Cannonball model's sphere radiuses, for matte and drum side of the foil, were determined to be:

$$r_{\_matte} \approx 0.06 R_{z\_matte} \approx 0.06 \times 2.13 \approx 0.128\mu m$$

$$r_{\_drum} \approx 0.06 R_{z\_drum} \approx 0.06 \times 2.50 \approx 0.150\mu m$$

Because most EDA tools only allow a single value for the radius parameter, the average radius (r_{avg}) was determined to be:

Equation 15

$$r_{avg} = \frac{r_{\_matte} + r_{\_drum}}{2} \approx \frac{0.150 + 0.128}{2} \approx 0.139 \mu m$$

Polar Instruments Si9000e [5] was the primary tool used for this case study because it is a popular tool used by many board shops for designing stackups. It has a simple user interface which helps getting the answer quickly, with less chance of mistake.

As mentioned earlier, it includes the Cannonball-Huray model, so all that was needed was to enter R_z for drum and matte side after etch treatment from Table 3, then the other roughness parameters were automatically computed, simplifying the whole procedure.

The wideband causal dielectric model option was used to model dielectric properties over frequency. Effective D_k due to roughness for core and prepreg, calculated above, were substituted instead of data sheet values.

After the transmission lines were modeled and simulated, the S-parameter results were saved in touchstone format. Keysight ADS [6] was used for further simulation analysis and comparison.

Figure 9 compares the simulated results vs measurement of a 5inch, de-embedded stripline trace. The red plots are measured and blue plots are simulated. Differential IL is shown on the left and differential phase delay is shown on the right. As can be seen, there is excellent correlation for IL but measured phase delay at 10 GHz is higher than simulated.

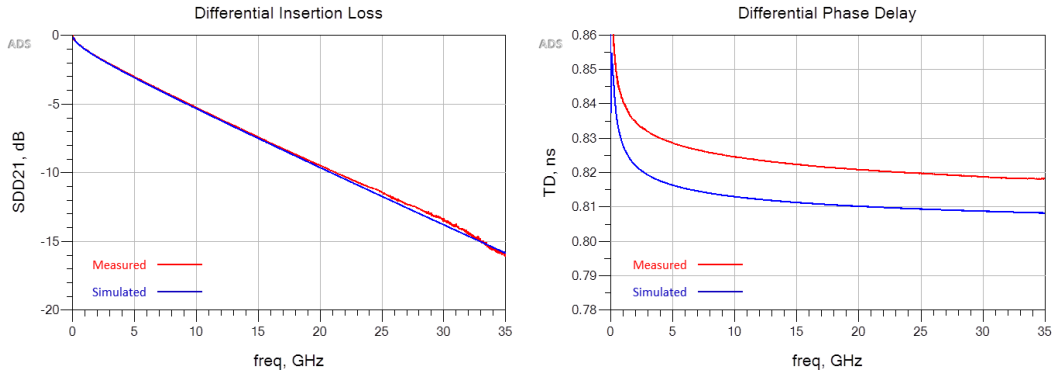


Figure 9 Measured (red) vs simulated (blue) insertion loss (left) and phase delay (right).

D_{keff} can be derived from phase delay. This is also known as time delay (*TD*) and is often used as a metric for simulation correlation accuracy for phase. *TD*, as a function of frequency, in seconds, is calculated from the unwrapped measured transmission phase angle, and is given by [20]*:

Equation 16

$$TD(f) = -1\left(\frac{unwrap(phase(S21))}{360 \times freq}\right)$$

* Keysight ADS equation syntax[6]

and:

D_{keff}, as a function of frequency, is then given by:

Equation 17

$$D_{keff}(f) = \left(TD(f) \frac{c}{Length} \right)^2$$

where:

c = speed of light (m/s)

Length = length of conductor (m)

Results for D_{keff} due to roughness are shown in Figure 10. On the left graph, D_{keff} measured at 10 GHz was 3.787, compared to simulated 3.511, which was 7.8% higher when data sheet values were used. But when the respective D_{keff_rough} was used, the measured result was only 2.9% higher, as shown on the right graph.

Although D_{keff} is closer, to measurements, it is non-causal because the roughness correction factor has only been applied to the real part of the internal impedance of the metal. This is evident by the difference in shape between the two curves, especially less than 10 GHz

In our DesignCon 2018 paper [21], we showed that when the roughness correction factor was also applied to the imaginary part of the internal impedance of the metal, it corrects the inductance due to roughness and improves the simulated transmission line characteristics.

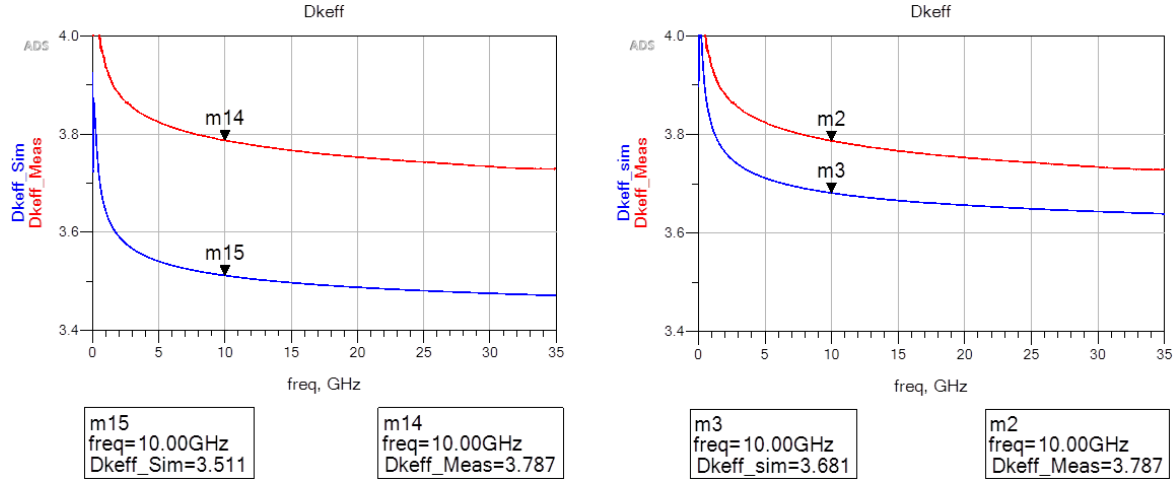


Figure 10 Measured (red) vs simulated (blue) D_{keff} using Meg-4 data sheet values for core and prepreg (left) and using D_{keff_rough} (right).

Simbeor's Huray-Bracken roughness model [22] was then used to compare the causal and non-causal conductor model differences. The model requires two parameters; Roughness Factor (*RF1*) and Surface Roughness (*SR1)* as shown in Figure 11.

The average sphere radius, r_{avg} = 0.139 μm from Equation 15 was entered for *SR1* and then used in Equation 18 below to determine *RF1*.

Equation 18

$$RF1 = 1 + \frac{3}{2}\left(\frac{N4\pi r^2}{A_{flat}}\right) = 1 + \frac{3}{2}\left(\frac{14 \cdot 4\pi (r_{avg})^2}{36(r_{avg})^2}\right) \approx 8.33$$

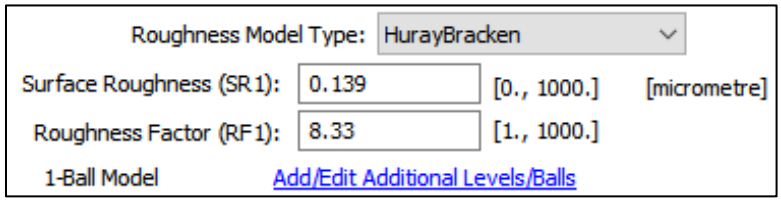


Figure 11 Simbeor's Huray-Braken causal roughness model parameter panel.

After modeling and simulation the transmission line geometry, the resulting S-parameters were saved in touchstone format and then brought into Keysight ADS [6] for further analysis. The results are shown in Figure 12.

When the causal version of conductor roughness model was applied, simulated D_{keff} matches measurements almost exactly. This is remarkable, considering there was no additional tuning or curve fitting parameters from manufacturers' data sheet values!

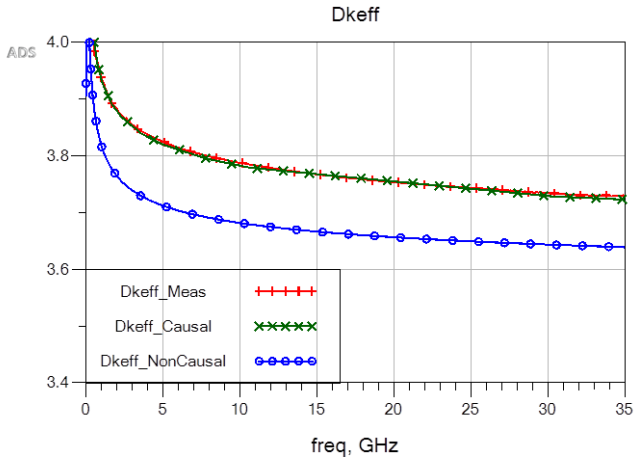


Figure 12 D_{keff} corrected due to roughness and complex roughness correction factor applied.

Figure 13 shows simulated vs measured results for time domain transmission (TDT) single bit response (SBR) on the left and time domain reflectometry (TDR) on the right. The SBR shows the causal model is almost an exact fit to measurements. Both have more delay due to the increased inductance. But even though the non-causal SBR shows slight differences in rise and fall time shape, the result suggests the non-causal model is still useful.

The TDR impedance shows that even though the exact stripline cross-section geometry is unknown, both simulations are within 10% of measurements. Etch factor of the trapezoidal traces alone, can explain the variation.

The causal model has higher characteristic impedance and the rising slope is a better match to measured results. Nevertheless, the non-causal model is still useful.

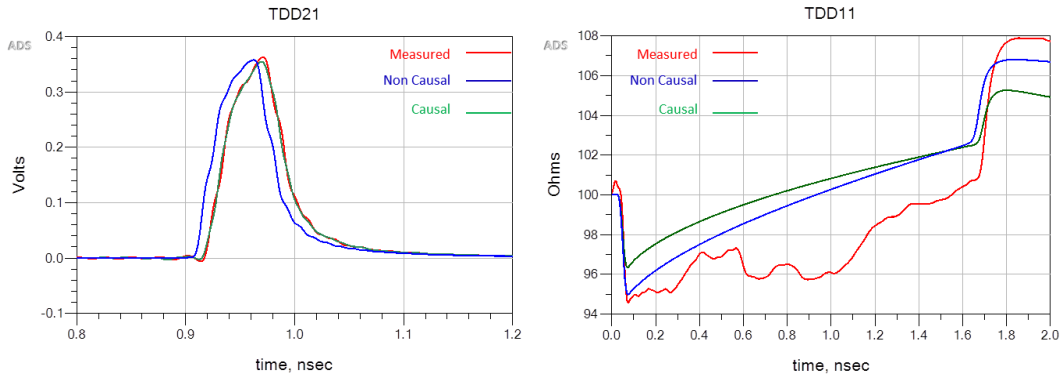


Figure 13 Causal / non-causal vs measured time domain transmission (TDT) single bit response (left) and time domain reflected (TDR) response (right).

Impact of OA on Insertion Loss & Impedance

In 2016 the High-density Packaging User Group (HDPUG) [16] undertook a project to evaluate the high frequency loss impacts of a variety of OA treatments on a Megtron-6 (Meg-6) test platform using HVLP base foil on core laminates prior to lamination. OA treatments studied included: older chemical etch bonding treatments; newer low etch bonding treatments; and non-etch bonding treatments. The paper [17] was published and presented at APEX 2017 conference. Some measured results, shown in Table 2, were used in this paper to study the impact of OA on insertion loss and impedance.

A total of 10 samples from each of the six OA treatments were measured with a Zygo 7100 optical surface profiler. The average RMS roughness (R_q) measurements from each are summarized in Table 2 [17]. Samples A and B are older etch treatments. Sample C is a low etch treatment, while samples D, E and F are newer OA treatments that promote adhesion without chemical etching.

Figure 14 are scanning electron microscope (SEM) photos, credit [16], of existing OA etch treatment samples. A typical roughness profile for samples A B C is shown on the left and newer non-etch OA treatments, D E F, is shown on the right. As can be seen the underlining surface profile of the smooth surface is maintained using the non-etch treatment with slight increase in RMS roughness compared to base copper roughness.

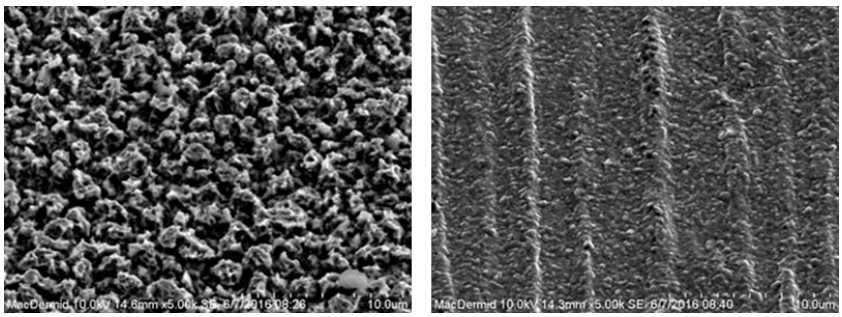


Figure 14 SEM pictures of existing OA etch treatments (left) and newer non-etch OA treatments (right). Photo credit [16].

To understand what the impact of different OA treatments have on IL, a simple simulation test case was set up using Polar SI9000e field solver [5]. Material chosen for the study was Meg-6K with 0.5 oz HVLP foil. Matte side R_z roughness for HVLP was 1.5 μm, as reported by Panasonic's data sheet. R_q from respective OA treatments [17] were converted to R_z using Equation 7 in order to use the Cannonball-Huray model.

Engineering data sheet values for D_k @ 12GHz were 3.38 and 3.20 for core and prepreg respectively. They were subsequently adjusted due to roughness for each OA sample using Equation 1 and all are summarized in Table 2.

Table 2 Comparison of R_q copper surface roughness measurements after OA treatment [17] and summary of D_{keff} due to roughness.

Sample	OA *Rq** (μm)	OA *Rz*** (μm)	Matte *Rz* (μm)	D_{keff} Core @12GHz	D_{keff} Prepreg @12GHz	D_f @12GHz
Base CU	**0.3050**	1.0566	1.5000	3.4856	3.2541	0.004
A	**0.5470**	1.8949	1.5000	3.4856	3.2984	0.004
B	**0.5480**	1.8983	1.5000	3.4856	3.2986	0.004
C	**0.4400**	1.5242	1.5000	3.4856	3.2787	0.004
D	**0.2860**	0.9907	1.5000	3.4856	3.2507	0.004
E	**0.3170**	1.0981	1.5000	3.4856	3.2563	0.004
F	**0.3130**	1.0843	1.5000	3.4856	3.2556	0.004

* Ref [17]; ** $R_z \approx R_q(2\sqrt{3})$ per Equation 7

The differential pair stripline geometry chosen is summarized in Figure 15. Er1, Er2 are the effective dielectric constant parameters for core and prepreg respectively. They were adjusted accordingly for each sample per Table 2. REr is the dielectric constant of mostly resin of prepreg in between the traces.

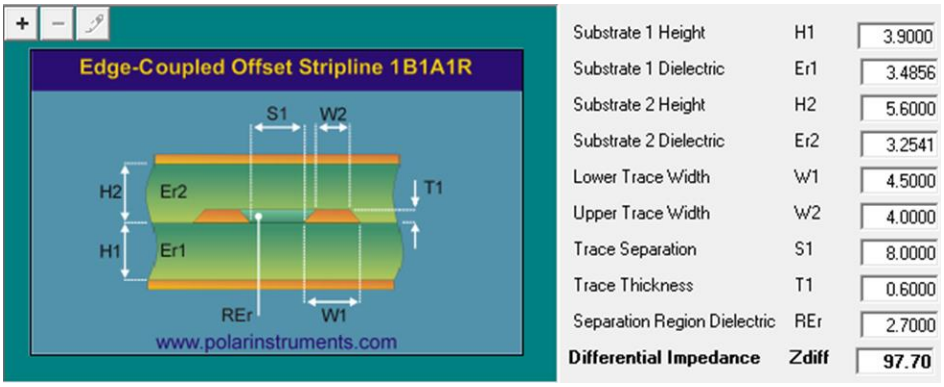


Figure 15 Differential pair stripline geometry used for OA study input to Polar SI9000e field solver [5].

Figure 16 summarizes simulated IL per inch for each sample. As expected the smoother the roughness shows improvement in insertion loss especially extending to 50 GHz with the best improvement coming from samples D, E and F which are the newest class of OA treatments that promote adhesion without chemical etching.

At 14GHz there is 0.07 dB/inch delta between OA sample B and sample D. At 28GHz this delta increases to 0.16dB/inch. This suggests that for the current 56 GB/s standards, OA is probably not that much of an issue; as long as the OA etch treatment is tightly controlled by the PCB fabricator. But for future 112GB/sec standards it could be an issue; depending on what part of the compliance spec you are trying to meet.

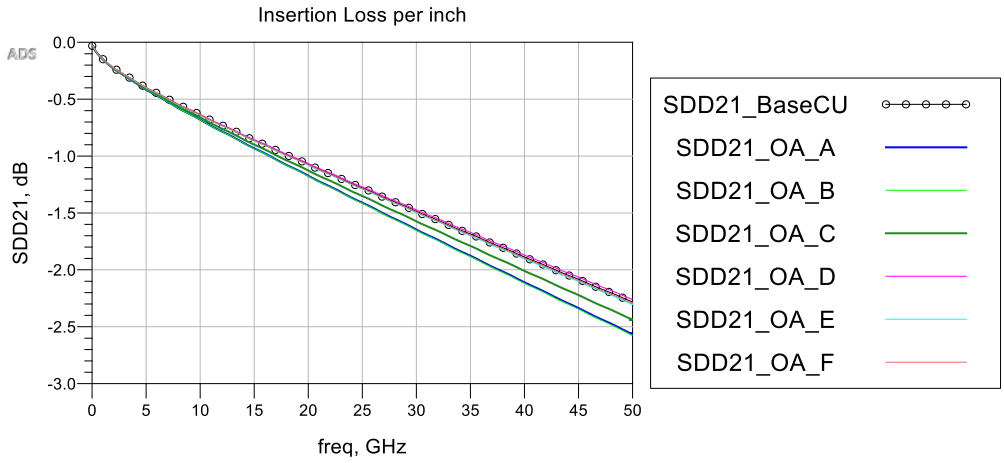


Figure 16 Summary of SDD21 per inch vs OA treatment.

Figure 17 Summarizes differential impedance. As can be seen, the rougher the OA treatment, the lower the impedance. This is expected because of the higher D_{keff} due to the roughness.

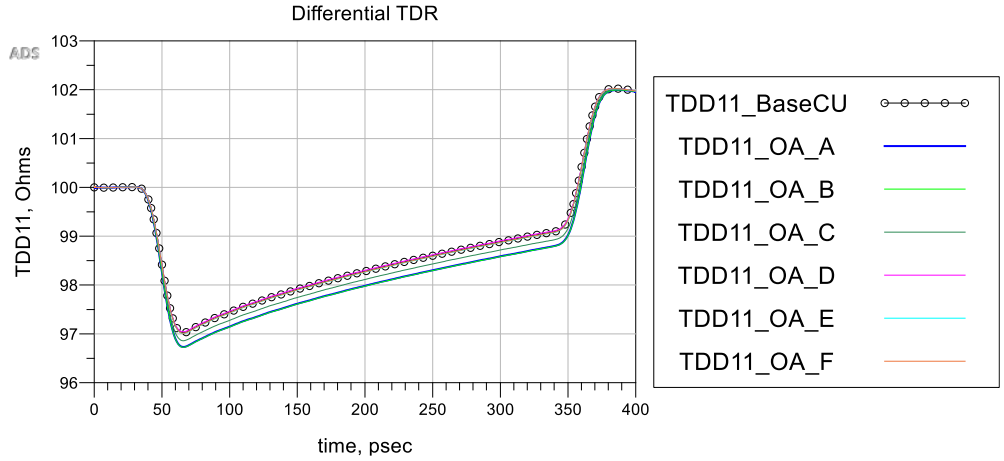


Figure 17 Summary of TDD11 vs OA treatment.

Practical Channel Modeling of a High-speed Backplane Case Study

A traditional high-speed serial link backplane channel model has three separate parts. They are two plug-in circuit daughter cards (DC) and a backplane (BP). Neglecting vias, the high-speed channel can be quickly modeled as three separate transmission line segments with connectors in-between.

The best way to demonstrate this is through a practical case study example. An Amphenol-FCI Examax [23] demo platform, I co-designed along with FCI and Via Systems back in 2013, shown in Figure 18, was used.

Figure 18 Amphenol-FCI Examax demo platform and channel topology summary used for case study.

The DCs were identical with all differential pairs of equal lengths. Among other test structures designed into the BP, there were four channels with different overall lengths. For simplicity only one channel topology shown in Figure 19 was used for comparison in this case study.

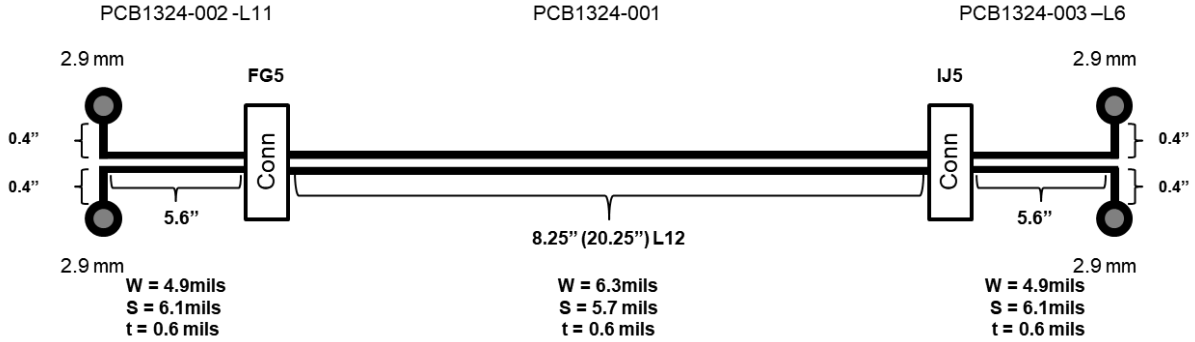


Figure 19 Topology of backplane case study.

The PCBs were fabricated with Nelco N4000-13epsi material [8]; clad with MW-G-VSP foil from Oak-mitsui [9]. OA treatment used was sample C from Table 2. The respective transmission line design and data sheet parameters are summarized in Table 3.

Table 3 Design parameters and data sheet summary

Parameter	**N4000-13EPSI Backplane**	**N4000-13EPSI Daughter Card**
D_k Core/Prepreg @ *10GHz*	3.08/3.06	3.04/3.06
D_f Core/Prepreg @ *10GHz*	0.0083/0.0084	0.0085/0.0084

Parameter	N4000-13EPSI Backplane	N4000-13EPSI Daughter Card
R_z Matte side	2.5 μm	2.5μm
R_z Drum side with OA	1.5 μm	1.5 μm
Trace Thickness, t	0.6 mils (15.2 μm)	0.6 mils (15.2 μm)
Trace Width, w_1	6.3 mils (160.0μm)	4.9 mils (124.5 μm) (Diff) 5.4 mils (137.2 μm) (SE)
Trace Width, w_2	5.7 mils (144.8 μm)	4.3 mils (109.2 μm) (Diff) 4.8 mils (121.9 μm) (SE)
Trace Separation, s	5.7 mils (144.8 μm)	6.1 mils(154.9 μm)
Core thickness, H1	6 mils (152.4 μm)	4 mils(101.6 μm)
Prepreg thickness, H2	6.2 mils (157.5 µm)	6.2 mils(157.5 µm)

The first step was to determine D_{keff} due to roughness for the cores and prepregs used on the DC and BP.

Daughter Cards:

$$D_{keff\_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_drum}\right)} \times D_{k\_prepreg} = \frac{157.5\mu m}{\left(157.5\mu m - 2\times 1.5\mu m\right)} \times 3.06 = 3.12$$

$$D_{keff\_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_matte}\right)} \times D_{k\_core} = \frac{101.6\mu m}{\left(101.6\mu m - 2\times 2.5\mu m\right)} \times 3.04 = 3.20$$

Backplane:

$$D_{keff\_prepreg} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_drum}\right)} \times D_{k\_prepreg} = \frac{157.5\mu m}{\left(157.5\mu m - 2\times 1.5\mu m\right)} \times 3.06 = 3.12$$

$$D_{keff\_core} = \frac{H_{smooth}}{\left(H_{smooth} - 2R_{z\_matte}\right)} \times D_{k\_core} = \frac{152.4\mu m}{\left(152.4\mu m - 2\times 2.5\mu m\right)} \times 3.08 = 3.18$$

Each transmission line segment was modeled separately using Polar Si9000e field solver [5]. The respective D_{keff} due to roughness for core and prepreg were entered into the causal dielectric model for DC and BP geometries. Since Polar uses the Cannonball-Huray model, R_z for both matte and drum sides were entered directly. Sphere radius, r_{avg} and A_{flat} were then automatically computed.

For each length of transmission line of the topology, shown in Figure 19, three separate S-parameter files were generated and saved in touchstone format. One file was the single-ended traces on the DC. Another one was for the differential pair on the DC and the last one was for the differential pair on the BP.

Keysight ADS [6] was then used to model and simulate the entire backplane channel. The schematics are shown in Figure 20. Fig. A schematic was used for frequency domain analysis, while Fig. B was used for transient channel simulation. All the S-parameter files from Polar were concatenated together, including the Examax connector. Vias and 2.9 mm co-ax connectors were not modeled.

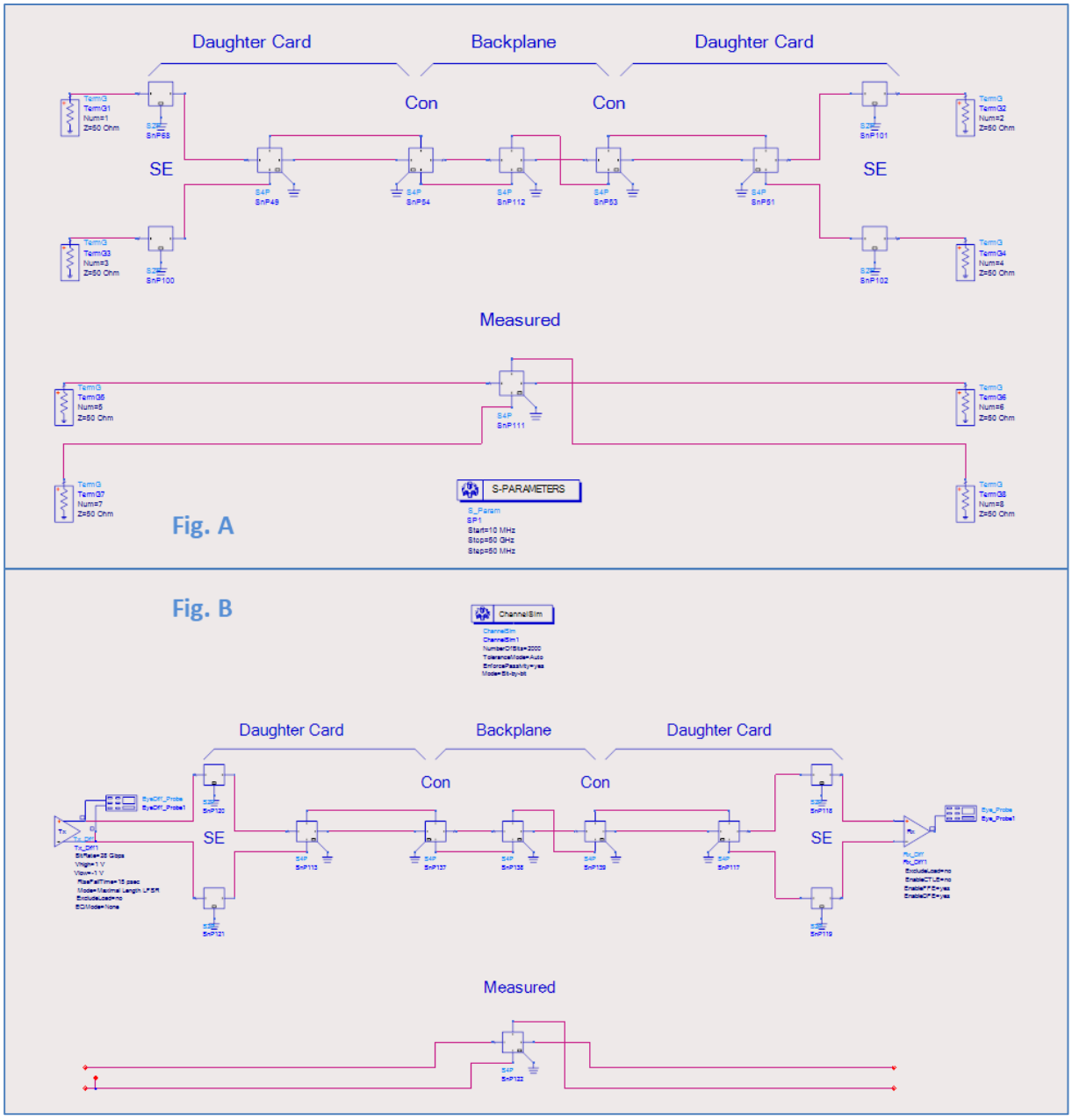


Figure 20 Keysight ADS generic topology models for frequency domain (Fig. A) and transient channel simulation analysis (Fig. B).

The results of the simulations are plotted in Figure 21. Differential insertion loss (SDD21) is shown on the left and differential TDR (TDD11) is shown on the right.

Since IEEE802.3bs [27] specifies a data rate of 53.12 GB/s (26.56 GBd/s), IL at 13.28 GHz Nyquist frequency is -21.8dB vs -20.8dB for the simulated and measured channels respectively. As can be seen, there is excellent correlation for both; considering the simplicity of the channel model and ONLY using data sheet parameters.

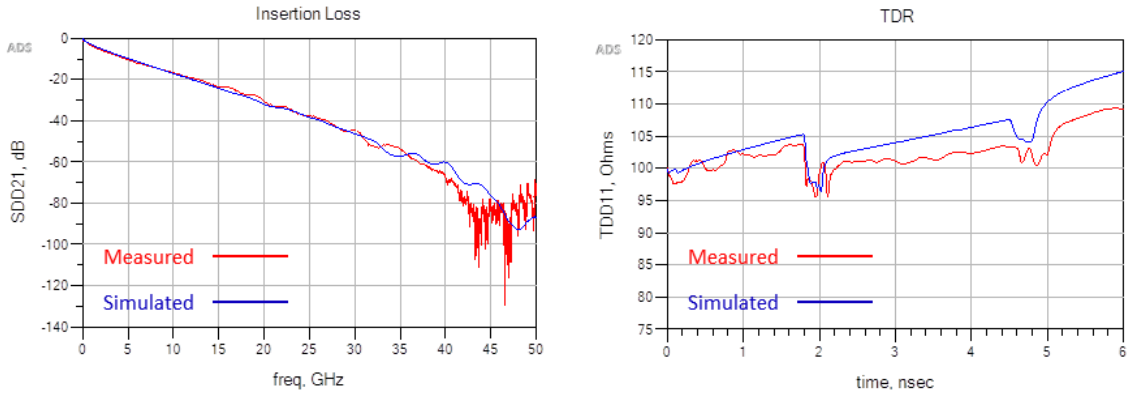


Figure 21 Measured vs simulated differential insertion loss (SDD21) shown on left and differential TDR (TDD11) shown on right.

Figure 22 shows results for the transient channel modeling simulations. The simulated channels are shown on the left and the measured channels are shown on the right. Transmit eyes are on top and receive eyes are on the bottom.

IBIS-AMI back channel interface (BCI) models used were courtesy of Keysight Technologies [6]. A short stress pattern random quaternary (SSPRQ) [27] test pattern was used for the bit pattern. Eye width and height measurements were measured at bit error ratio (BER) of 10^{-6}.

As can be seen, the measured channel transmit eye has more noise due to reflections causing an average height reduction of 12% across all three eyes at the receiver. This was expected since vias and 2.9mm coax connectors were not included in the channel model. Surprisingly though, there was only a 3% increase in jitter averaged across all three eyes.

Even though the measured channel show slightly more noise and jitter the "*OK answer NOW!*" model is still useful and maybe good enough to make certain engineering decisions or risk assessments.

Summary and Conclusions

By using Cannonball-Huray model, with copper foil roughness and dielectric material properties obtained solely from manufacturers' data sheets, practical PCB interconnect modeling for high-speed design is now achievable using commercial field-solving software employing Huray model.

The non-causal model for conductor loss does not adversely affect simulation results when compared to measurements and shouldn't disqualify EDA tools that have not included a causal metal loss model.

Acknowledgements

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- Hugues Tournier, from Ciena Corporation for s-parameter measurements and stackup details for the Meg-4 test PCB used for the case study.
- Heesoo LEE, from Keysight Technologies for the IBIS-AMI PAM-4 BCI models and help with setting up the back-channel simulations.

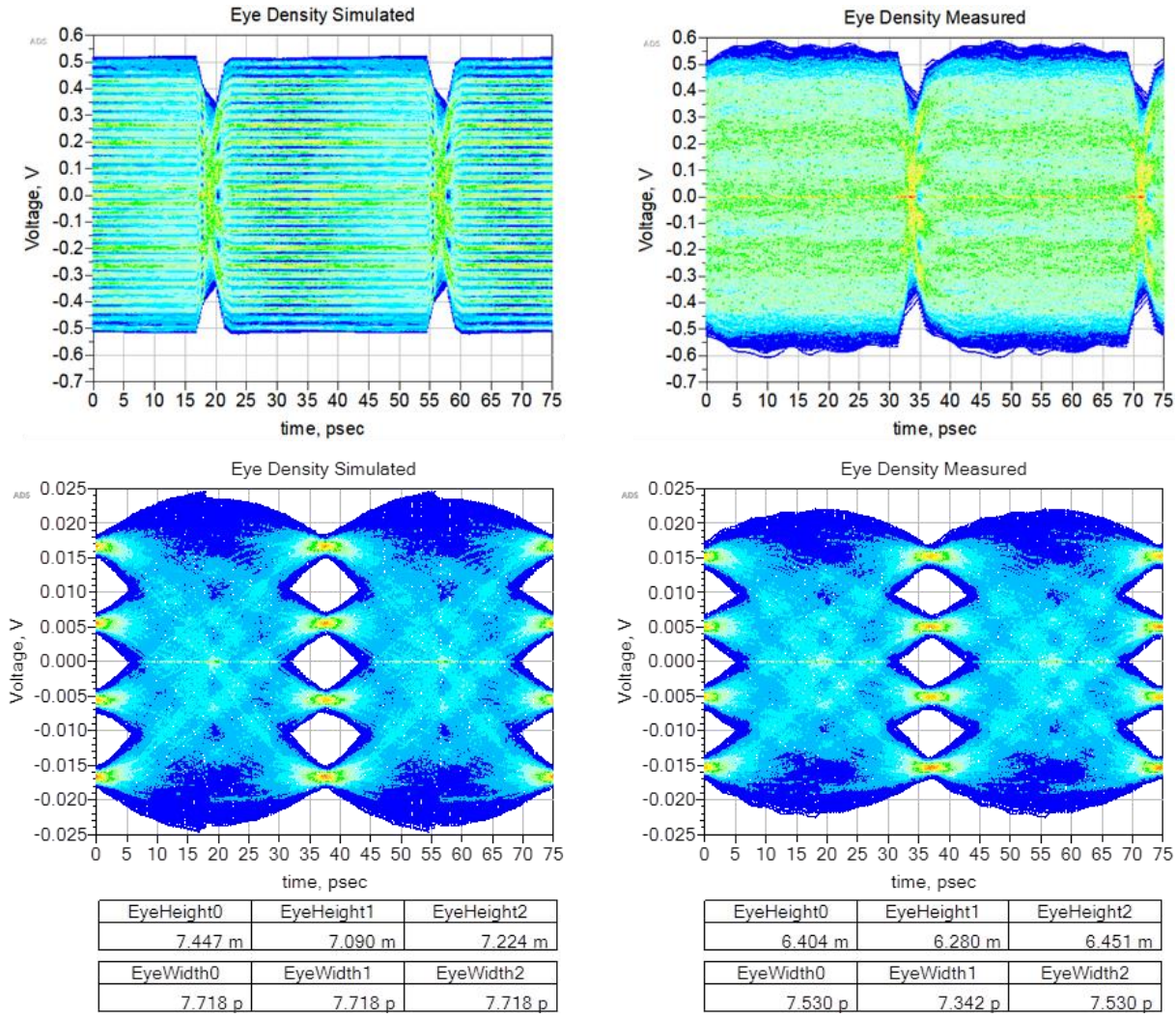

Figure 22 IEEE802.3bs PAM-4 channel simulation comparison (left) to measurements (right) at 53.12 GB/s. Total length = 20.25". Top plots are at transmitter. Bottom plots are at the receiver output after equalization. Measurements are receive eye heights and widths at 10^{-6} BER.

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