# White Paper

## Method of Modeling Differential Vias

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## Abstract

Accurate, models for vias in a multilayer circuit board are necessary to predict link performance in the GHz regime. This paper describes a methodology to build a high bandwidth, scalable first approximation circuit model using simple transmission lines of long vias typically used in thick backplane designs. System architects and backplane designers for example can quickly model various interconnect topologies for what-if scenarios and to set the direction for a more detailed design evaluation. It includes necessary parameters to study and quantify the through and stub effects when effective dielectric constant and via impedance are varied. As an added benefit, this simple modeling technique also provides a means to validate and sanitize later models built with 3D field solvers when users have a limited skill set in the use of the tools.

# Author's Biography

Lambert (Bert) Simonovich graduated in 1976 from Mohawk College of Applied Arts and Technology in Hamilton, Ontario, Canada as an Electronic Engineering Technologist. Over a 32 year career at Bell Northern Research and Nortel, he helped pioneer several advanced technology solutions into products and has held a variety of R&D positions, eventually specializing in backplane design over the last 25 years. He is the founder of Lamsim Enterprises Inc. www.Lamsimenterprises.com providing innovative signal integrity and backplane solutions. He is currently engaged in signal integrity, characterization and modeling of high speed serial links associated with backplane interconnects. He holds two patents, two IEEE publications and co-author of an award winning DesignCon2009 paper related to via modeling.

Eric Bogatin received his BS in physics from MIT and MS and PhD in physics from the University of Arizona in Tucson. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft and Interconnect Devices. Eric has written 4 books on signal integrity and interconnect design and over 200 papers. His latest book, Signal and Power Integrity- Simplified, was published in 2009 by Prentice Hall. He has taught over 4,000 engineers in the last 20 years. Many of his papers and columns are posted on the www.BeTheSignal.com web site.

Yazi Cao received the B.S. and Ph.D. degrees in electrical engineering from Wuhan University, Hubei, China, in 2004 and 2008, respectively. His research interests include neural network, design and modeling of RF/Microwave circuits.
Since 2009, he has been a postdoctor in the Department of Electronics, Carleton University, Ottawa, Canada.

# Record of Changes:

Issue 1.0 -April 8, 2010 – Initial release
Issue 2.0 -January 17, 2011 - Page 14, the equation directly above (16) 3.60E-9 corrected to actually read 3.60E+3.
Issue 2.1-January 25, 2011- Page 32 – Corrected typo in equation $fo_2$ to read 20.2GHz and corrected *fo* equation below with 2.02E10.
Issue 2.2-April 2, 2012 – Page 32 – Corrected typo in equation *Dkeff2* denominator to 0.126

# Introduction

Present integrated circuit (IC) technology advancements are allowing data rates in excess of 10 Gb/s. PCB through hole via parasitics are becoming more of a factor affecting bit error rate (BER) performance. Accurate via modeling for topology simulations are a must and often require sophisticated 3D modeling tools.

Most of these tools are complex, expensive and require a high level of expertise to operate. With corporate R&D budgets shrinking, board design engineers are required to take on more diverse responsibilities. In many cases, they lack the necessary skill set and or expertise to use sophisticated modeling tools properly because they lack the time to invest in learning it properly, or they uses the tool too infrequently. Personal experience has proved mistakes can happen when drawing or inputting parameters leading to inaccurate results. Often there are no simple methods to sanitize the results especially if there are no measurements available that can be used for model sanitization.

Behavioral models and circuit topology models are two generic kinds of models used to simulate high speed serial links. S-parameters are called behavioral models because they describe the behavior of the structure with respect to incident waveforms from calibrated ports. They can be used as a behavioral representation of the actual structure once the device is measured.

Measured S-parameter behavioral models are limited because they represent everything connected between the calibrated reference planes of the VNA. Elaborate de-embedding and calibration schemes are needed to remove fixture effects from the measurement to leave behind just the s-parameter's structure of interest. Even then, they represent only one sample of a given construction. It is impossible to perform what-if, worst case min/max analysis with a single behavior model. Their usefulness in model development is to help build, calibrate and validate circuit topology models.

A circuit topology model on the other hand, is a schematic representation of the structure. When run in a circuit simulator, it predicts a measureable performance of the structure. These models can be parameterized so that worst case, min/max analysis can be explored quickly. For any physical structure, there can be more than one circuit topology that describes it. All can give the same performance, up to some bandwidth.

This work is part of a follow-up study from the DesignCon2009 paper "Practical Analysis of Backplane Vias", by Bogatin, Simonovich, Gupta and Resso [5]. Our goal of this paper was to develop an analytical methodology and equations to develop a circuit topology model of a differential via structure in the absence of measured data. The model should be simple, yet match the measured performance up to a high bandwidth. It should be validated against a 3D field solver and correlated back to measured results.

# Anatomy of a Differential Via Structure

An example of a differential via structure through a printed circuit board (PCB) stack-up is shown in Figure 1. It is representative of vias used to connect surface mounted components or backplane connectors to internal layer traces as opposed to vias used to transition between layers when signals are routed between inner layers. It forms the basis of a via modeling methodology presented in this paper

The via barrel is a plated through hole extending the entire length of a PCB stack-up. The outside diameter equals the drill diameter. The inside diameter is the finished hole size (FHS) after plating. Pads are used on layers to ensure there is sufficient copper for track attachment after drilling operation. When used in this fashion, they are referred to as "functional" pads. Anti-pads are the clearance holes of plane layers to prevent shorting to the via barrel or pads.

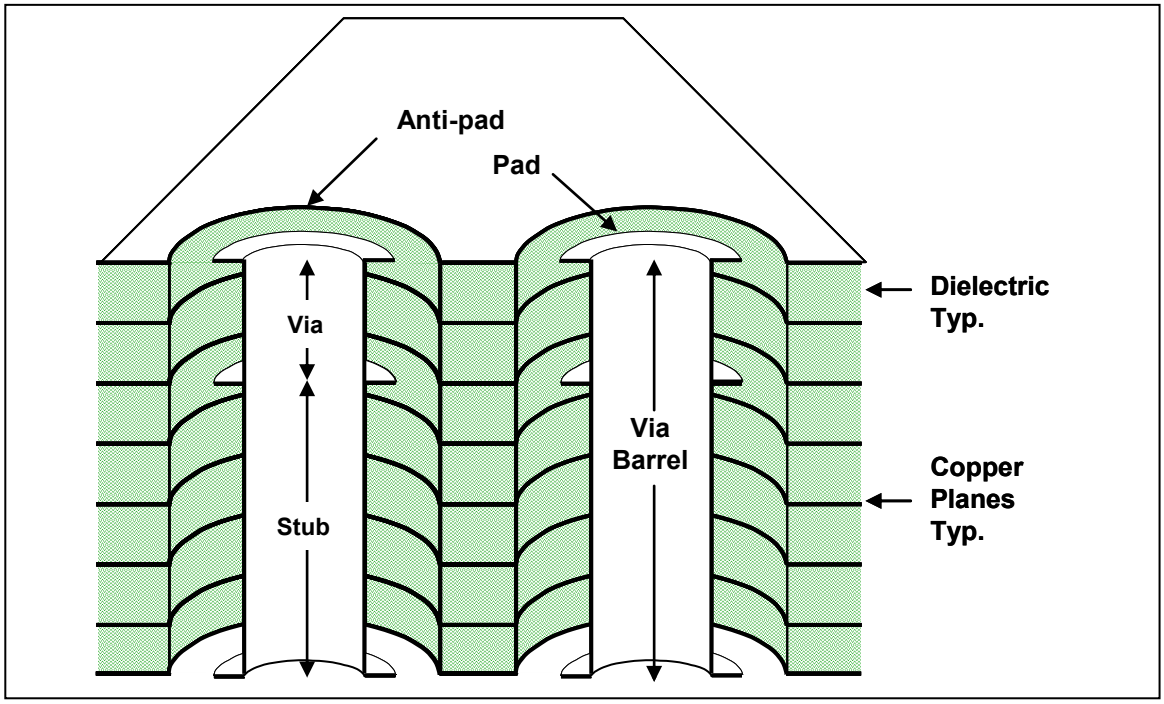



**Figure 1 Differential Via Structure Through a Multilayer PCB**

The via portion is the length of the via barrel connecting one signal layer to another. It is often referred to as the through via since it is part of the signal net. The stub portion is the remainder of the via barrel extending to the outer layer of the PCB. In high speed designs where the via stub is greater than 300mils/BR, where BR is the bit rate in Gb/s, it can be the primary cause of signal degradation and eye closure [6].

High speed point-point serial link based backplanes are often thick structures due to the system architecture and card-card interconnect requirements. Back-drilling the via stub is common practice on thick PCBs to minimize stub length for bit rates greater than 3Gb/s.

Conventional FR4 type laminates are fabricated with a weave of glass fiber yarns and resin. The effective dielectric constant (Dk) is a function of glass to resin ratio of the laminate used for the PCB stack-up. When a signal propagates in a stripline fashion through a fiberglass reinforced laminate, the electric field is in the z-axis and orthogonal with respect to the surface of the board. However, when a signal propagates through a pair of vias driven differentially, the electric field is in the x-y axis and sees a different combination of glass weave and resin content with different distributions as illustrated in Figure 2. This makes the material anisotropic in nature. Dankov et al [4] has shown the effective dielectric constant in the x-y axis can be 15-20% higher than the z axis.

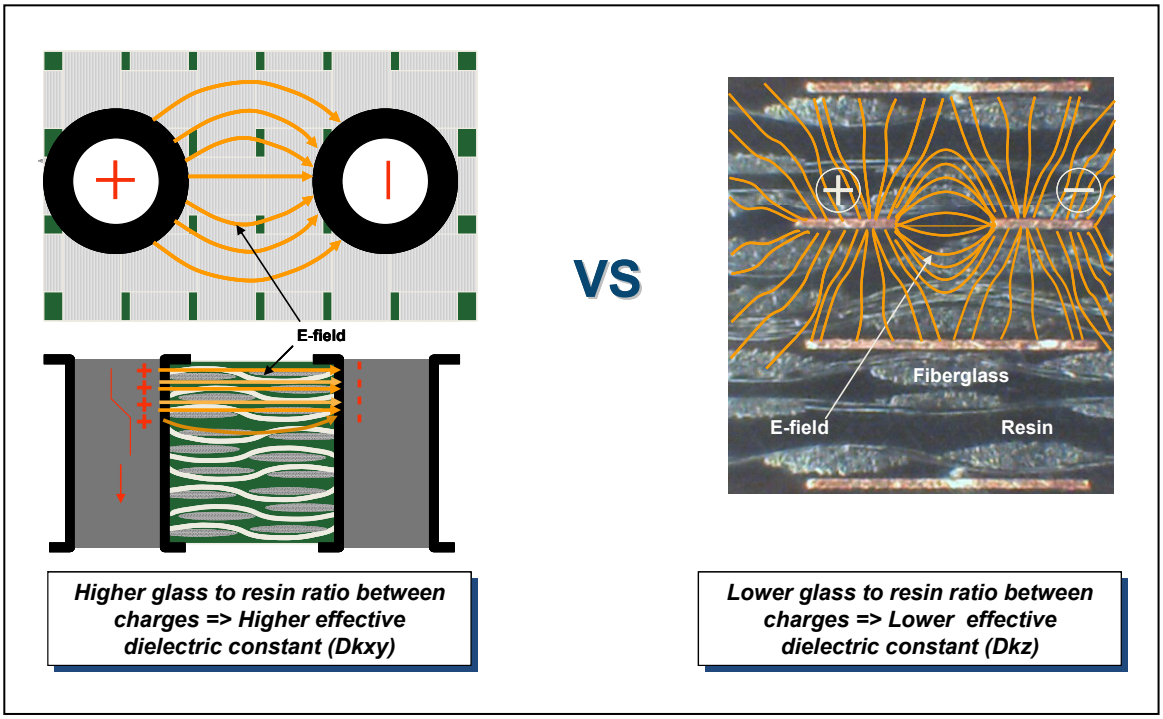



**Figure 2 Electric field direction in the laminate of the two different regions. Between via barrels (left) and in the stripline interconnect (right)**

The differential via structure can be represented by a twin-rod transmission line geometry. The distributed excess capacitance over its entire length is due to the via barrel`s proximity to the anti-pads. The smaller the anti-pad diameter, the greater the distributed excess capacitance will be. This ultimately results in lower via impedance thereby increasing reflections. In all high speed serial link designs, it is common practice to remove all non-functional pads and to maximize the anti-pad clearance as much as practically possible. Oval anti-pads are often used in this regard to further mitigate excess via capacitance.

## Twin-Rod Transmission Line Geometry

A twin-rod transmission line geometry as illustrated in Figure 3 is one of three cross-sectional geometries that have exact equations for characteristic impedance. The other two geometries are coaxial and rod-over-plane. All three relationships assume the dielectric material is homogeneous and completely fills the space whenever there are electric fields.

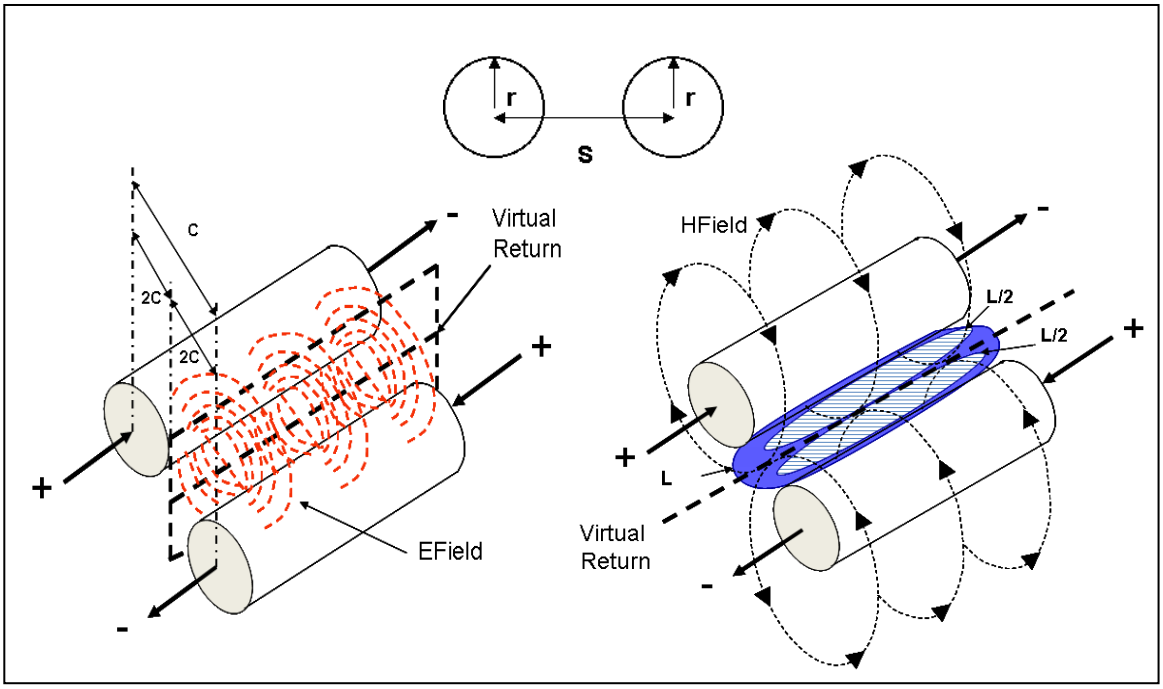



**Figure 3 Twin-rod geometry showing electro-magnetic field relationship**

The relationships between capacitance, inductance and impedance of twin-rod geometry are described by the following equations:

$$Ctwin = \frac{7.06E-13}{\ln\left(\frac{s}{2r}\left[1+\sqrt{1-\left(\frac{2r}{s}\right)^2}\right]\right)} \times Dk \times Len \qquad \textbf{(1)}$$

$$Ltwin = 10.16E-9 * \ln\left(\frac{s}{2r}+\sqrt{\left(\frac{s}{2r}\right)^2-1}\right) * Len \qquad \textbf{(2)}$$

$$Zdiff = \sqrt{\frac{Ltwin}{Ctwin}} = \sqrt{\frac{10.16E-9 * \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) * Len}{\frac{7.06E-13}{\ln\left(\frac{s}{2r}\left[1 + \sqrt{1 - \left(\frac{2r}{s}\right)^2}\right]\right)} \times Dk \times Len}}$$

$$Zdiff = \frac{120}{\sqrt{Dk}} \times \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \quad \textbf{(3)}$$

Where:

*Ctwin* = Capacitance between twin-rods - F
*Ltwin* = Inductance between twin-rods – H
*Zdiff* = Differential impedance of twin-rods - Ω
*Dk* = Dielectric constant of material
*Len* = Length of the rods - inches
*r* = Radius of the rods - inches
*s* = Space between the rods - inches

When driven differentially, the electro-magnetic fields create a virtual return plane at exactly one half of the spacing between the rods. Each rod therefore behaves like a single rod-over-plane geometry.

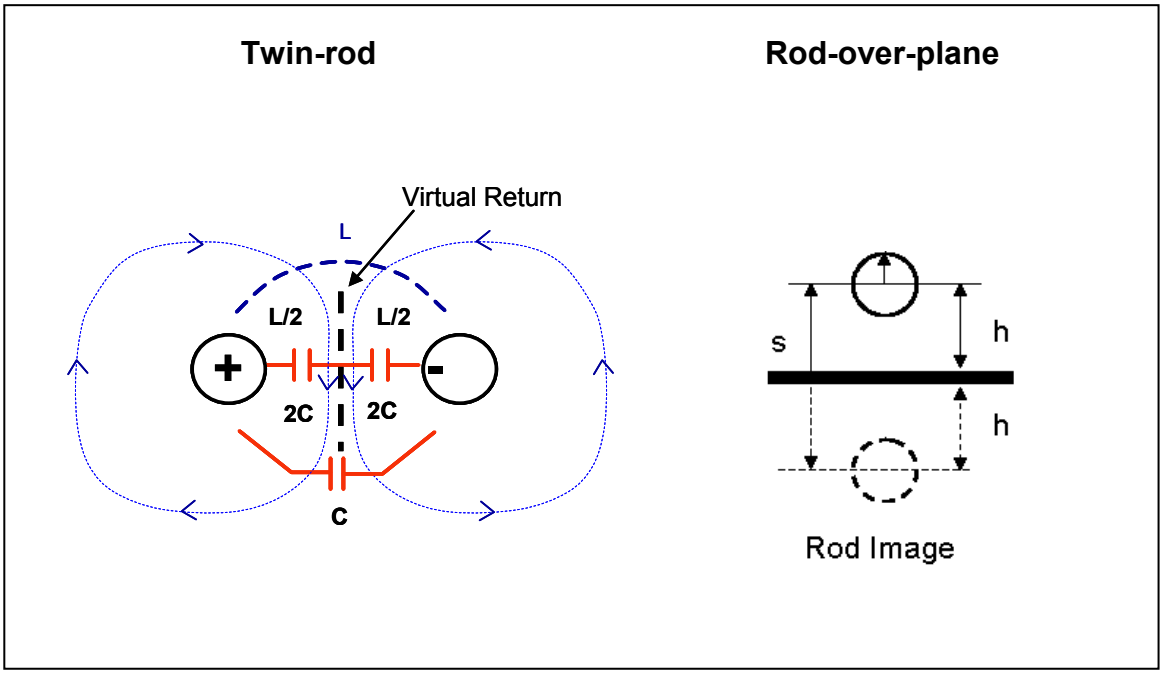



**Figure 4 Twin-rod vs Rod-over-plane**

The odd mode capacitance is the capacitance of each rod to virtual return plane and is equal to twice the capacitance between rods.

$$Codd = \frac{1.41E-12}{\ln\left(\frac{s}{2r}\left[1+\sqrt{1-\left(\frac{2r}{s}\right)^2}\right]\right)} \times Dk \times Len \qquad \textbf{(4)}$$

The odd mode inductance is the inductance of each rod to virtual return plane and equal to one half the inductance between rods.

$$Lodd = 5.08E-9 * \ln\left(\frac{s}{2r}+\sqrt{\left(\frac{s}{2r}\right)^2-1}\right) * Len \qquad \textbf{(5)}$$

The odd mode impedance of each rod is half of the differential impedance, and is equivalent to the rod-over-plane impedance.

$$Zodd = \sqrt{\frac{Lodd}{Codd}} = \frac{60}{\sqrt{Dk}} \times \ln\left(\frac{s}{2r}+\sqrt{\left(\frac{s}{2r}\right)^2-1}\right) \qquad \textbf{(6)}$$

## Coaxial Transmission Line Geometries

The coaxial transmission line geometry consists of a center conductor imbedded within dielectric material and surrounded by a continuous shield as illustrated in Figure 5. In this symmetrical structure, the electro-magnetic fields are contained within the shield.

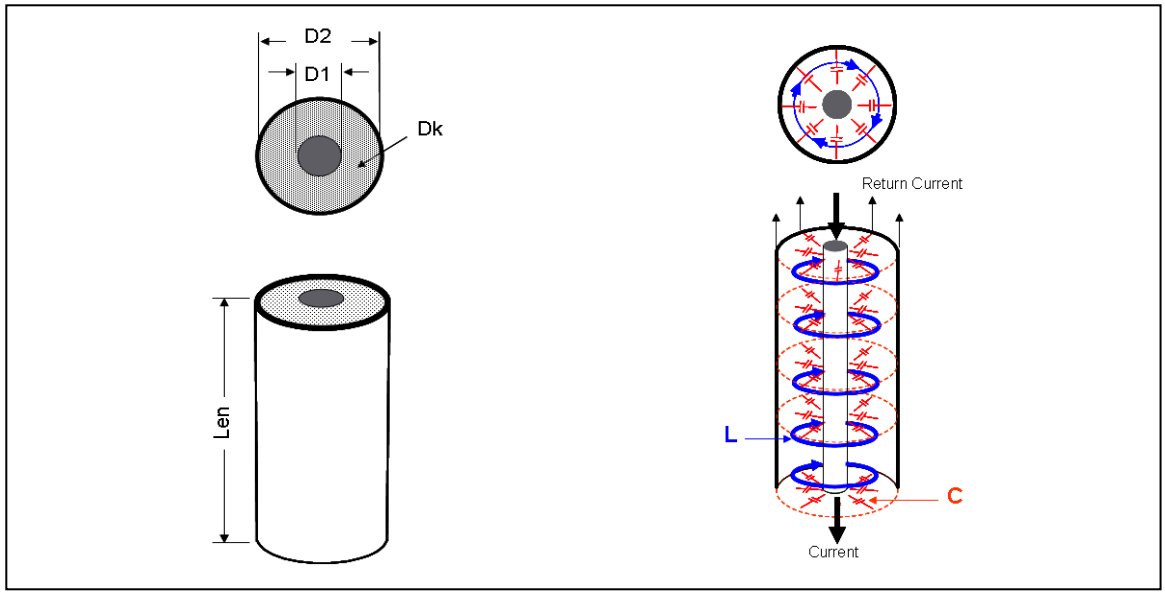



**Figure 5 Coaxial transmission line structure showing inductance (Blue) and capacitance (Red)**

The relationships between capacitance, inductance and impedance of coaxial geometries are:

$$Ccoax = \frac{1.41E-12}{\ln\left(\frac{D2}{D1}\right)} Dk \times Len \quad \textbf{(7)}$$

$$Lcoax = 5.08E-9 \times \ln\left(\frac{D2}{D1}\right) \times Len \quad \textbf{(8)}$$

$$Zo = \sqrt{\frac{Lcoax}{Ccoax}} = \sqrt{\frac{5.08E-9 \times \ln\left(\frac{D2}{D1}\right) \times Len}{\frac{1.41E-12}{\ln\left(\frac{D2}{D1}\right)} Dk \times Len}}$$

$$Zo = \frac{60}{\sqrt{Dk}} \times \ln\left(\frac{D2}{D1}\right) \quad \textbf{(9)}$$

Where:

*Ccoax* = Capacitance - F
*Lcoax* = Inductance – H
*Zo* = Characteristic Impedance - Ω
*Dk* = Effective Dielectric constant
*Len* = Length of the rods - inches
*D1* = Diameter of conductor - inches
*D2* = Diameter of shield - inches

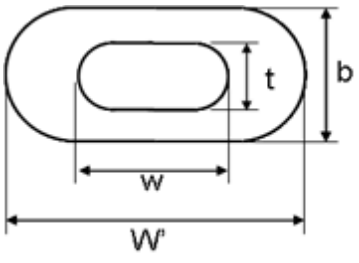



**Figure 6 Elliptic coaxial transmission line structure.**

An oval variation of a coaxial structure is a form of an elliptic coaxial structure shown in Figure 6. Gunston [8] derived the relationships between capacitance, inductance and impedance of elliptic coaxial geometries as:

$$Cellip \cong \frac{1.41E-12}{\ln\left(\frac{W'+b}{w+t}\right)} \times Dk \times Len \quad \textbf{(10)}$$

$$Lellip \cong 5.08E-9 \times \ln\left(\frac{W'+b}{w+t}\right) \times Len \quad \textbf{(11)}$$

$$Zo = \sqrt{\frac{Lellp}{Cellp}} \cong \sqrt{\frac{5.08E-9 \times \ln\left(\frac{W'+b}{w+t}\right)}{Dk \times \frac{1.41E-12}{\ln\left(\frac{W'+b}{w+t}\right)}}}$$

$$Zo \cong \frac{60}{\sqrt{Dk}} \times \ln\left(\frac{W'+b}{w+t}\right) \quad \textbf{(12)}$$

## Test Vehicle

The test vehicle used to correlate simulated results was the same one used in the DesignCon2009 paper [5]. Specifics are summarized in Figure 7.

The large dips in the insertion loss are a direct result of the ¼ wave resonance of the dangling stub. This resonant frequency is a good first order measure of the effective dielectric constant associated with the signal propagating down the stub. From the measured resonant frequency and the stub length, the effective dielectric constant can be estimated using the following equation;

$$Dkeff = \left[\frac{c}{4 * Stub\_length * f}\right]^2 \quad \textbf{(13)}$$

Where:

$c$ = Speed of light (1.18E10 inches/sec)
Stub_Length in inches
$f$ = ¼ wave frequency in Hz

Using the stub length of 270 mils and resonant frequency of 4.3 GHz, a Dkeff = 6.4, which matches the value extracted as the best fit of the parameterized model to the

measured data. Once the effective Dk was known, the odd-mode via impedance was easily calculated to be 32.5 Ω using the rod-over-plane impedance formula (6).

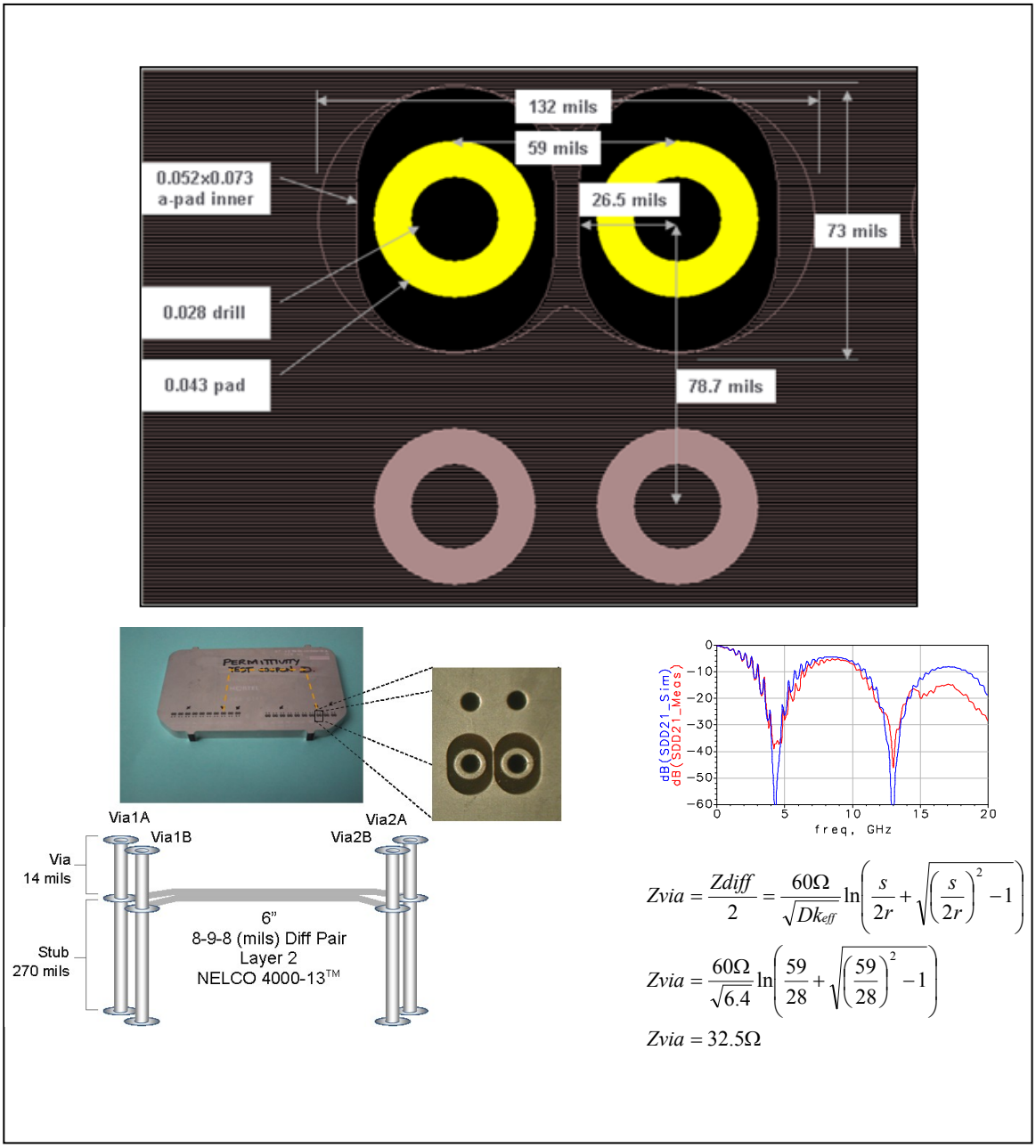



**Figure 7 Test vehicle summary from DesignCon2009 paper [5].**

## Building a Simple Scalable, Circuit Based Model

Our previous analysis [5] suggested a simple twin-rod model for a differential via transition, consisting of a uniform differential pair, can be used to accurately describe a

real differential via to very high bandwidth when calibrated to measured data. At the time of that publication, it was not possible to distinguish between a higher dielectric constant and a distributed capacitive loading due to coupling to the planes. It was thought the only way to distinguish these two effects was with a 3D field solver.

Since this work is a continuing study of differential vias, the model can be further simplified to use simple coupled transmission lines and setting the even mode parameters the same as the odd mode parameters as illustrated in Figure 8.

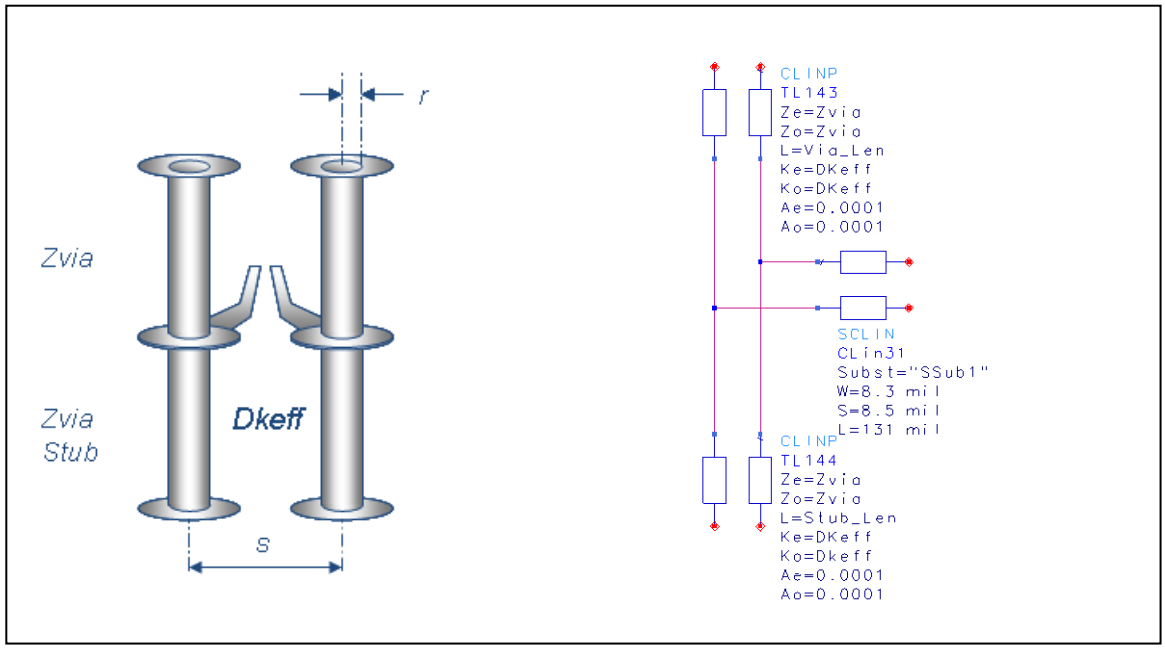



**Figure 8 Agilent ADS circuit based twin-rod via model.**

In a subsequent neural net via modeling paper by Cao, Simonovich and Zhang [7] a Dk_xy of 4.3 was used for an HFSS 3D model simulation of the same physical via structure. This value gave the best correlation to measurements. Part of that work showed the dielectric material had an anisotropic factor approximately 18% higher in the x-y axis over the average Dk in the z-axis. This corroborates well with Dankov et al's work [4] showing glass reinforced laminates have an anisotropic factor between 15-20%.

The work also helped answer previous questions we had in [5] and made it possible to distinguish between a higher effective dielectric constant and a distributed capacitive loading from coupling to the planes. In fact it turns out to be a little of both. It corrects a previous theory we had suggesting the effective dielectric constant in the x-y axis was predominated by the glass fiber density surrounding the via hole structure [3]. It is now possible to develop analytical equations for effective Dk and via impedance to be used in a parameterized circuit model.

## Developing Analytical Equations for $Dk_{eff}$ and $Z_{odd}$

A closer look at the anatomy of the differential the via structure under study is illustrated in Figure 9. Via capacitance is mainly influenced by the oval anti-pad.

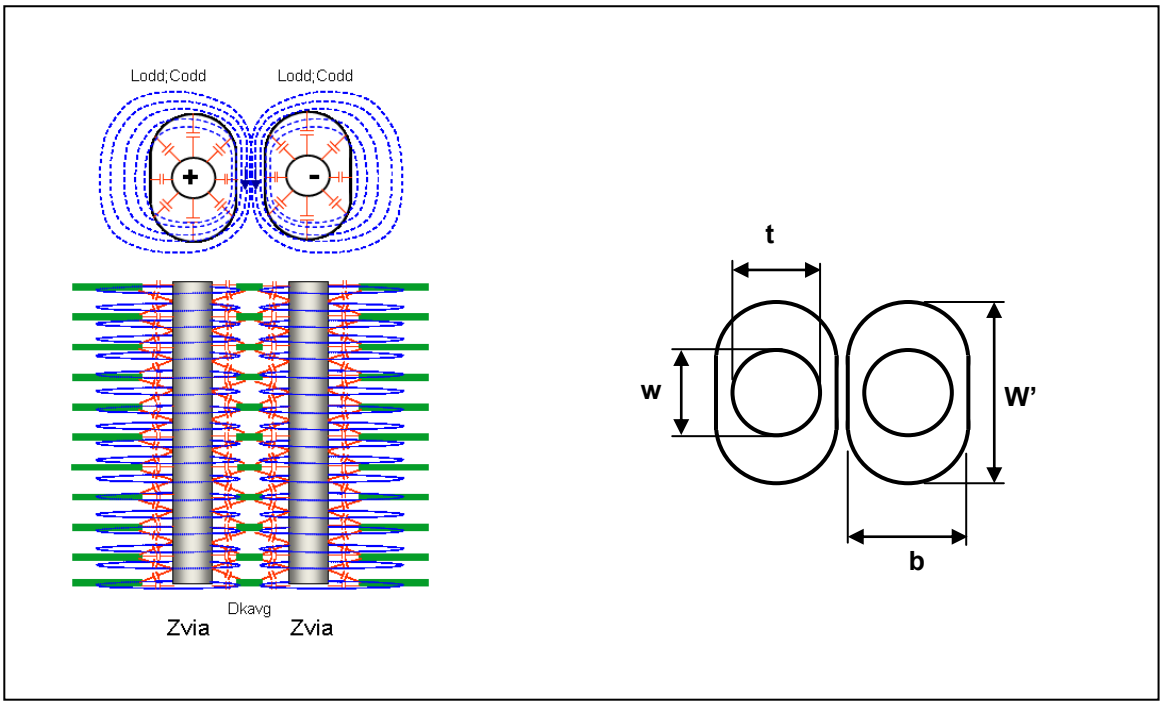



**Figure 9 EM Field relationship of twin-rod via model with oval anti-pads.**

Even though the shield is not continuous, the capacitance for each via surrounded by an oval anti-pad on the plane layers can be estimated using the elliptical coaxial transmission line equation (14). The thinner the dielectric between copper plane layers, the more accurate it will resemble a coaxial structure from an electrostatic point of view.

In order for the magnetic fields to behave like a coaxial structure, the shield must be continuous over the entire length. Since this is not the case, the magnetic fields behave more like a twin rod structure when the vias are driven differentially.

Therefore the odd-mode capacitance *Cvia* can be approximated as;

$$Cvia \cong \frac{1.41E-12}{\ln\left(\frac{W'+b}{w+t}\right)} \times Dkavg \times Len \qquad \textbf{(14)}$$

and the odd-mode inductance *Lvia* can be calculated as;

$$Lvia = 5.08E-9 \times \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times Len \qquad \textbf{(15)}$$

and the odd-mode impedance *Zvia* can now be approximated by;

$$Zvia \cong \sqrt{\frac{Lvia}{Cvia}} \cong \sqrt{\frac{5.08E-9 \times \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times Len}{Dkavg \times \frac{1.41E-12}{\ln\left(\frac{W'+b}{w+t}\right)} \times Len}}$$

$$Zvia \cong \sqrt{\frac{3.60E+3 \times \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+b}{w+t}\right)}{Dkavg}}$$

$$\boxed{Zvia \cong \frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+b}{w+t}\right)}} \qquad \textbf{(16)}$$

Where:

*Lvia* = Odd-mode via inductance - H
*Cvia* = Odd-mode via capacitance - F
*Zvia* = Odd-mode via impedance - Ω
*s* = via to via pitch – inches
*r* = radius of via barrel = Drill dia - inches

$$Dkavg = \frac{(Dkxy + Dkz)}{2}$$

$\left(\frac{W'+b}{w+t}\right)$ = Oval dimensions per Figure 6

The bulk dielectric constant *Dkavg* is due to the combination of resin and glass weave distribution. If a differential signal is propagated between the twin rods, it would see this bulk dielectric constant. However, it also sees the capacitive loading from the fringe

fields between the barrel and the planes it passes through. This distributed capacitance effectively lowers the odd-mode impedance of the via and increases the effective dielectric constant.

The effective dielectric constant can be evaluated based on how much the via's odd-mode impedance is decreased. Based on the twin rod formula, the via's odd-mode impedance can be expressed as;

$$Zvia = \frac{Ztwin}{2} \cong \frac{60}{\sqrt{Dkeff}} \times \sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)}$$

Substituting the odd-mode impedance from equation (16) into the equation above, and solving for *Dkeff* yields;

$$Dkeff = \left[\frac{60}{Zvia} \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)\right]^2$$

$$Dkeff = \left[\frac{60}{\left(\frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+b}{w+t}\right)}\right)} \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)\right]^2$$

$$Dkeff = \left[\frac{\sqrt{Dkavg}}{\sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+b}{w+t}\right)}} \ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)\right]^2$$

$$Dkeff = Dkavg \times \frac{\left[\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)\right]^2}{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+b}{w+t}\right)}$$

$$Dkeff = Dkavg \times \frac{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)}{\ln\left(\frac{W'+b}{w+t}\right)} \quad \textbf{(17)}$$

# Model Parameter Validation Using 2D and 3D Field Solvers

The model's accuracy was compared against Quickfield 2D [9] and Ansoft HFSS 3D [10] field solvers to study the effects of anti-pad variation in capacitance and Dkeff respectively. In order to remove any ambiguity of anisotropic factor from the dielectric, a Dk = 1 was used in all field solver and analytical equations. For both scenarios, the anti-pad dimensions were varied from 0.053"x0.053" round to ovals where the oval length was varied in 5 mil increments up to 0.080" long.

## Quickfield Capacitance and Inductance Correlation

Figure 10 shows the electrostatic plot and equipotential lines distribution of round vs oval coaxial structures. As the oval increases in length, the equipotential lines spacing become wider apart in the y-axis accounting for the reduced capacitance.

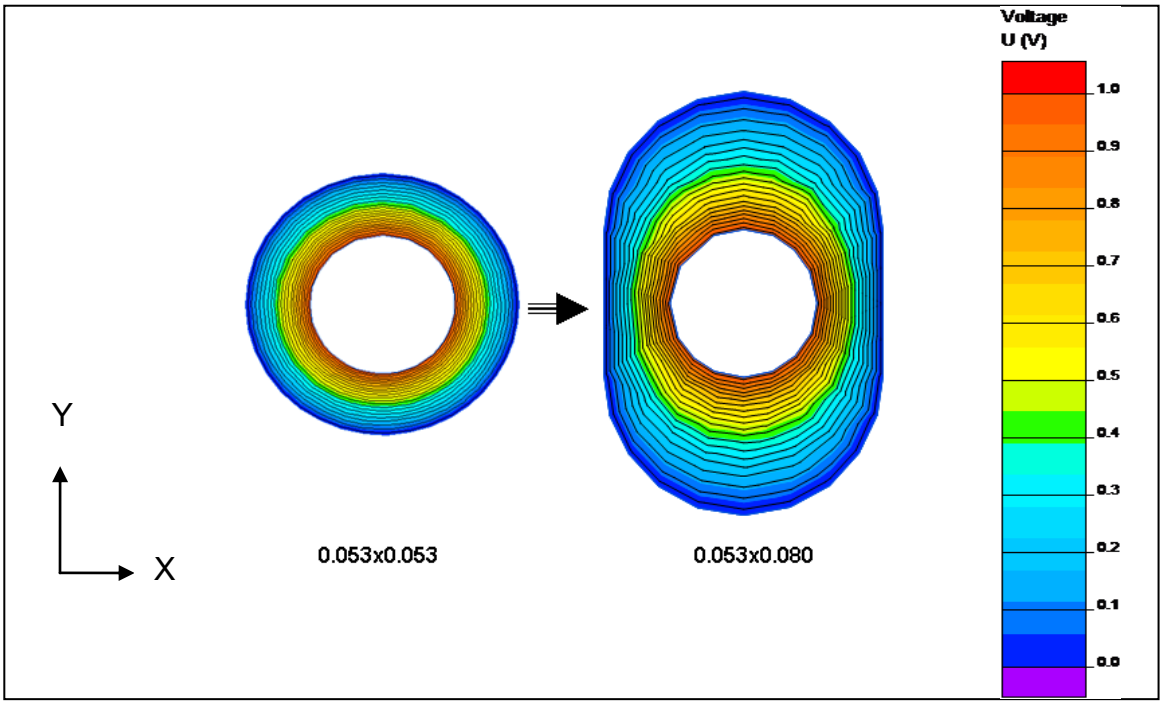



**Figure 10 Electrostatic field of circular vs oval shield. Dk = 1**

Using equation (14), via capacitance was calculated using Dk =1 for respective anti-pad variations. The results listed in Table 1 and plotted in Figure 11 in most cases show better than 2% correlation to Quickfield 2D field solver.

**Table 1 Comparison of Calculated Via Capacitance vs Quickfield 2D Field solver. Dk = 1**

| A-pad_W inch | A-pad_L inch | QuickField Capacitance F/in | Calculated Capacitance F/in | Delta% |
|---|---|---|---|---|
| | | | | |
| 0.053 | 0.053 | 2.19E-12 | 2.21E-12 | 1% |
| 0.053 | 0.055 | 2.10E-12 | 2.15E-12 | 2% |
| 0.053 | 0.060 | 1.98E-12 | 2.01E-12 | 1% |
| 0.053 | 0.065 | 1.85E-12 | 1.89E-12 | 2% |
| 0.053 | 0.070 | 1.79E-12 | 1.79E-12 | 0% |
| 0.053 | 0.075 | 1.70E-12 | 1.71E-12 | 0% |
| 0.053 | 0.080 | 1.65E-12 | 1.63E-12 | -1% |

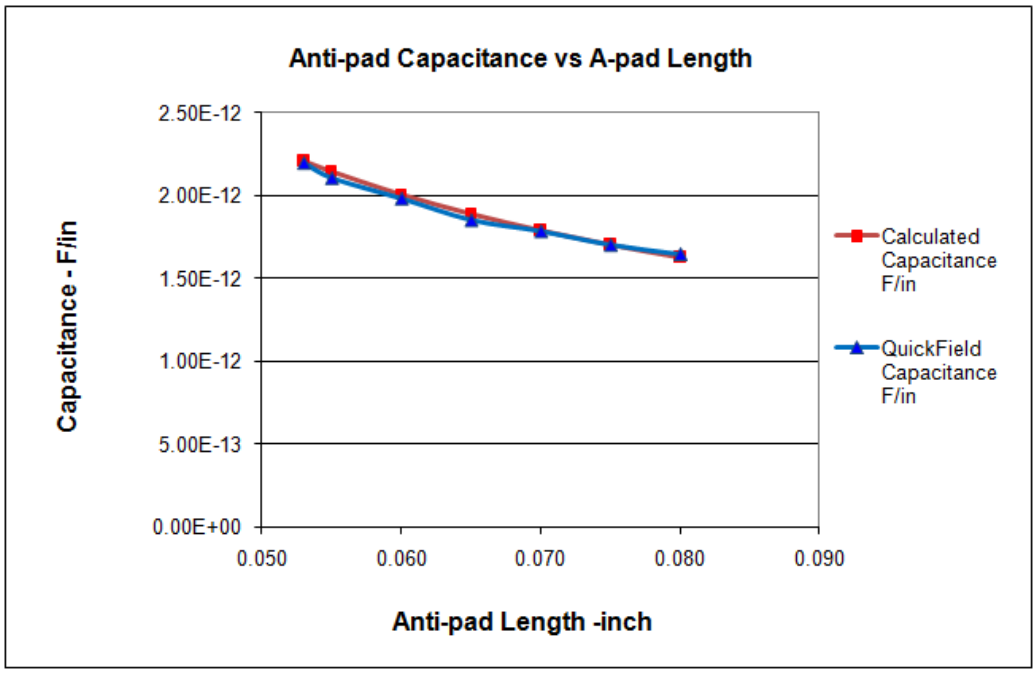



**Figure 11 Comparison of calculated vs Quickfield 2D field solver for via capacitance. Dk = 1**

Figure 12 shows the magnetic field relationship of a twin-rod via structure when driven differentially using Quickfield 2D field solver. The calculated odd-mode inductance using equation (15) was approximately 7nH compared to the Quickfield calculated 6.3nH. The discrepancy can most likely be attributed in part to the student version of software having a 255 node limitation for the mesh. The size of the model limits the mesh so accuracy is affected.

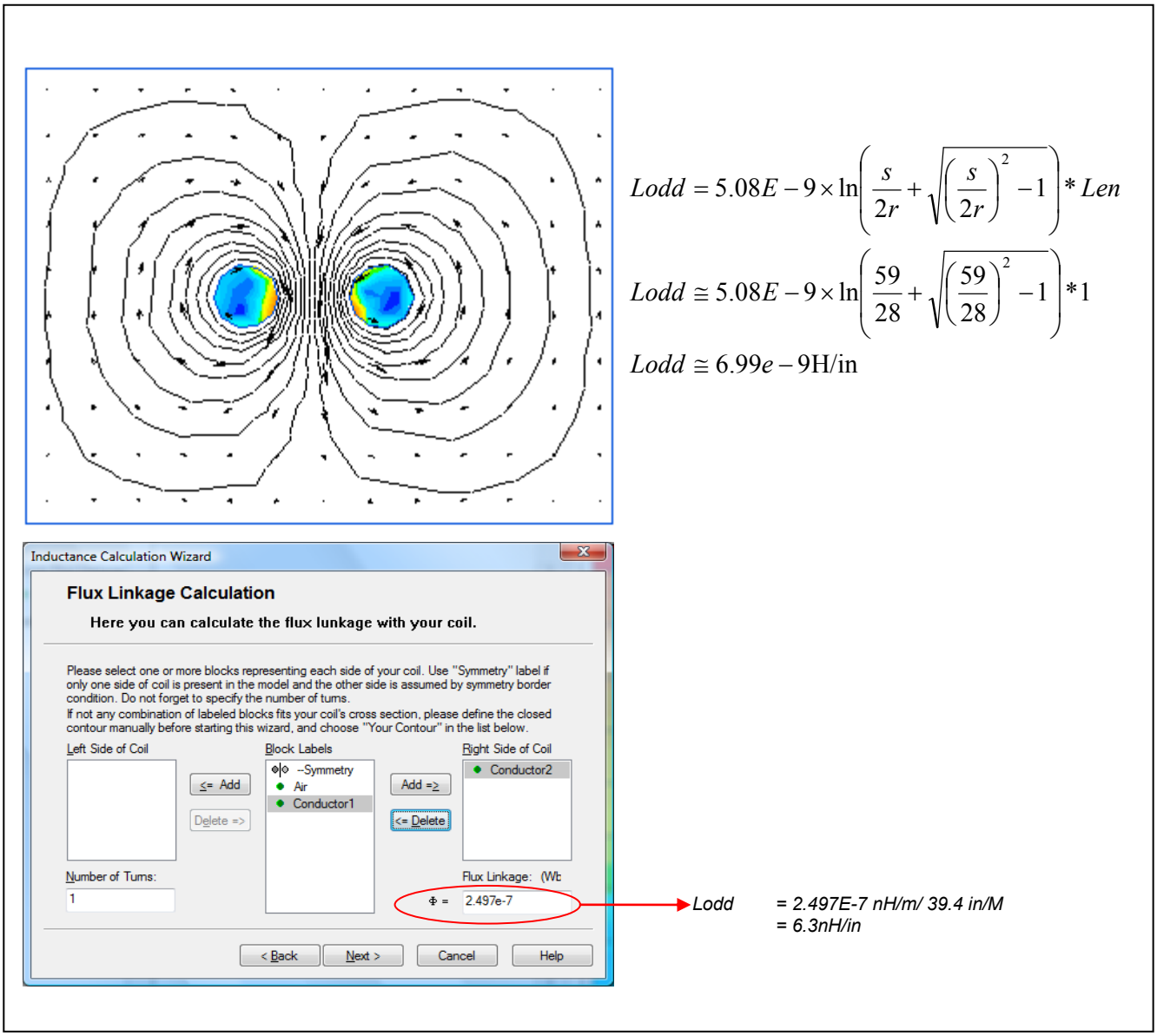
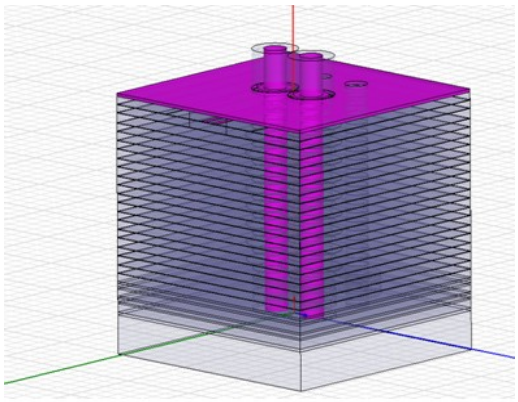
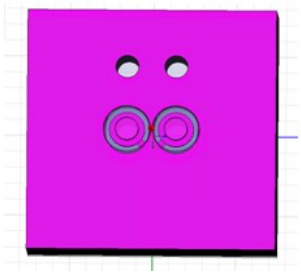
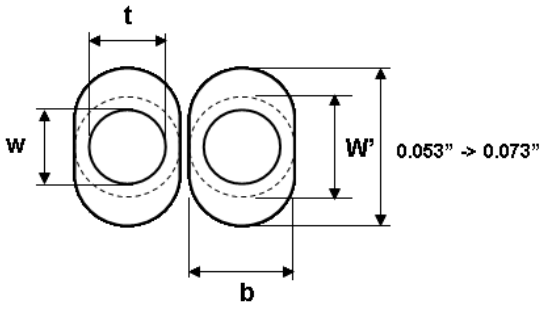



**Figure 12 Magnetic field twin-rod via structure. Simulated vs calculated inductance.**

## HFSS Dkeff Correlation








**Anti-pad Variation**

| b | W' | t | w |
|---|---|---|---|
| 0.053 | 0.053 | 0.028 | 0.028 |
| 0.053 | 0.055 | 0.028 | 0.028 |
| 0.053 | 0.060 | 0.028 | 0.028 |
| 0.053 | 0.065 | 0.028 | 0.028 |
| 0.053 | 0.070 | 0.028 | 0.028 |
| 0.053 | 0.075 | 0.028 | 0.028 |
| 0.053 | 0.080 | 0.028 | 0.028 |

**Figure 13 Ansoft HFSS model oval anti-pad variation. Dk=1**

The HFSS model shown in Figure 13 was developed for a neural net via modeling paper [7]. It was reused for this paper to validate the circuit model against Dkeff for various anti-pad lengths. The PCB stack-up dimensions used in the models were the nominal engineering specified values. A Dk = 1 was used as one of the model parameters for the simulation to simplify the analysis and remove any anisotropic ambiguity.

The equivalent via circuit model was then compared against the HFSS generated touchstone s-parameter file using Agilent ADS [11]. Both test topologies used for the simulations are shown in Figure 14. Ideal Balun transformers were used to simplify the display of differential s-parameters.

For each anti-pad dimension, a respective Dkeff was calculated based on the ¼ wave resonant frequency using equation (13) for each respective HFSS s-parameter file. The results are presented in Table 2, and plotted in Figure 15. They show excellent correlation to HFSS field solver results with less than 1% accuracy for oval anti-pad length to width ratios of less than 1.2:1, and 5% for 1.5:1 ratio.

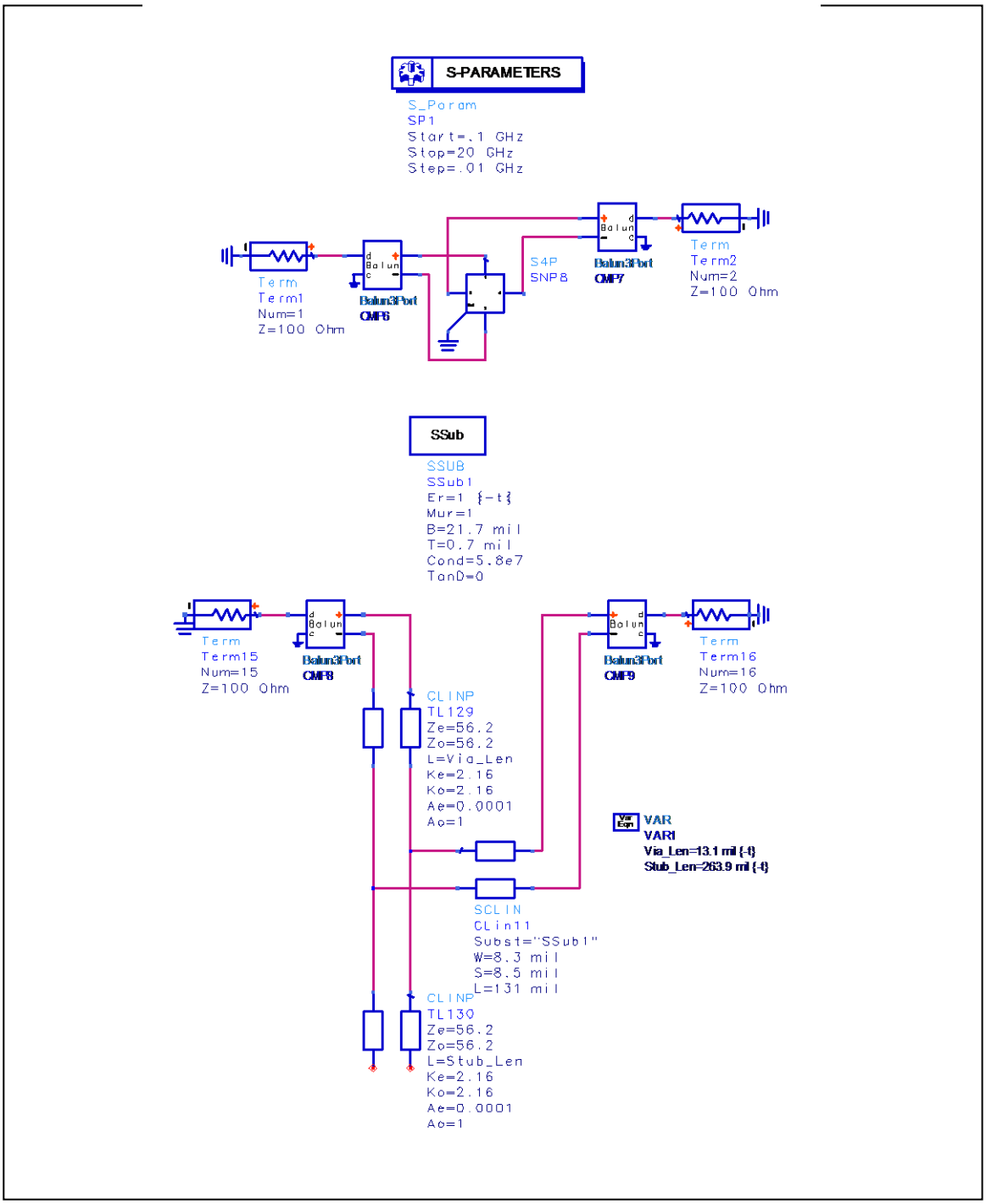



**Figure 14 HFSS touchstone S-parameter file (Dk=1) vs Agilent ADS test topology circuit model.**

**Table 2 Comparison of Dkeff calculated vs HFSS 3D field solver for Dk=1**

| Stub_Len inch | A-pad_W inch | A-pad_L inch | Res Freq HFSS Sim Hz | Dkeff_Sim HFSS | Dkeff_Cal Formula | Delta % | Zodd Cal ohms |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| 0.264 | 0.053 | 0.053 | 7.63E+09 | 2.15 | 2.16 | 0.5% | 56.2 |
| 0.264 | 0.053 | 0.055 | 7.75E+09 | 2.08 | 2.10 | 0.8% | 57.1 |
| 0.264 | 0.053 | 0.060 | 7.98E+09 | 1.96 | 1.96 | -0.1% | 59.0 |
| 0.264 | 0.053 | 0.065 | 8.19E+09 | 1.86 | 1.85 | -0.8% | 60.8 |
| 0.264 | 0.053 | 0.070 | 8.33E+09 | 1.80 | 1.75 | -2.8% | 62.4 |
| 0.264 | 0.053 | 0.075 | 8.43E+09 | 1.76 | 1.67 | -5.3% | 64.0 |
| 0.264 | 0.053 | 0.080 | 8.52E+09 | 1.72 | 1.59 | -7.5% | 65.5 |

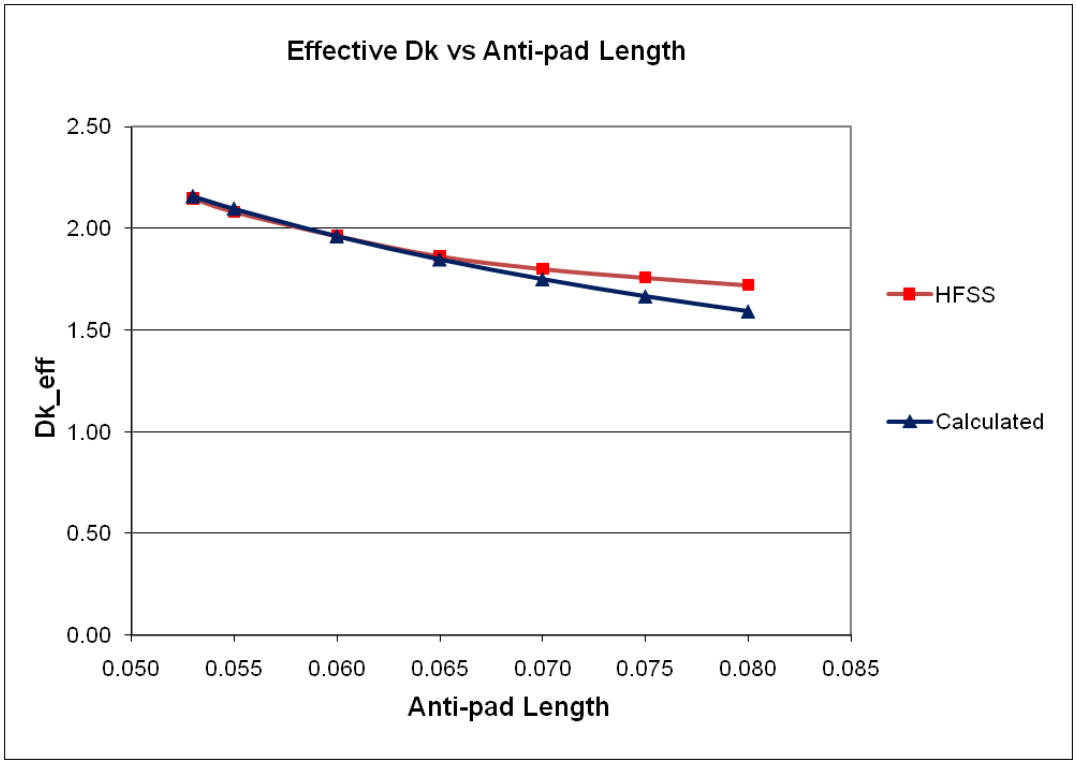



**Figure 15 Comparison of Dkeff calculated vs HFSS 3D field solver for Dk=1**

Comparing the insertion and return losses (Figure 16-Figure 22) shows excellent correlation for such a simple model. Table 3 summarizes the ¼ wave resonant frequency notches and shows the circuit model has better than 5% accuracy over the entire range of oval anti-pad variation.

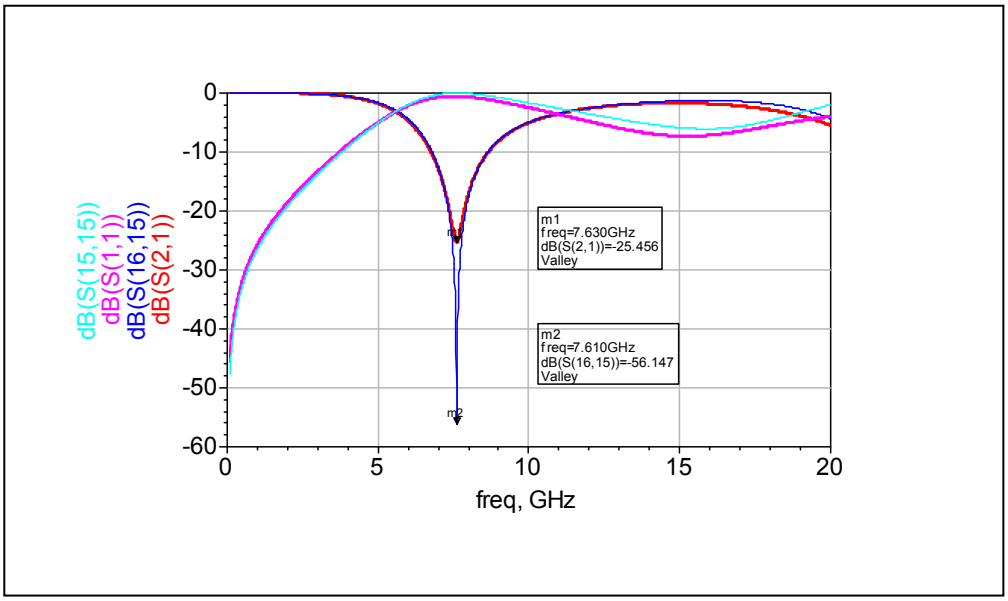



**Figure 16 |Comparison of insertion and return loss HFSS vs circuit model. Oval anti-pad; Dk = 1; Anti-pad = 0.053”x0.053”**

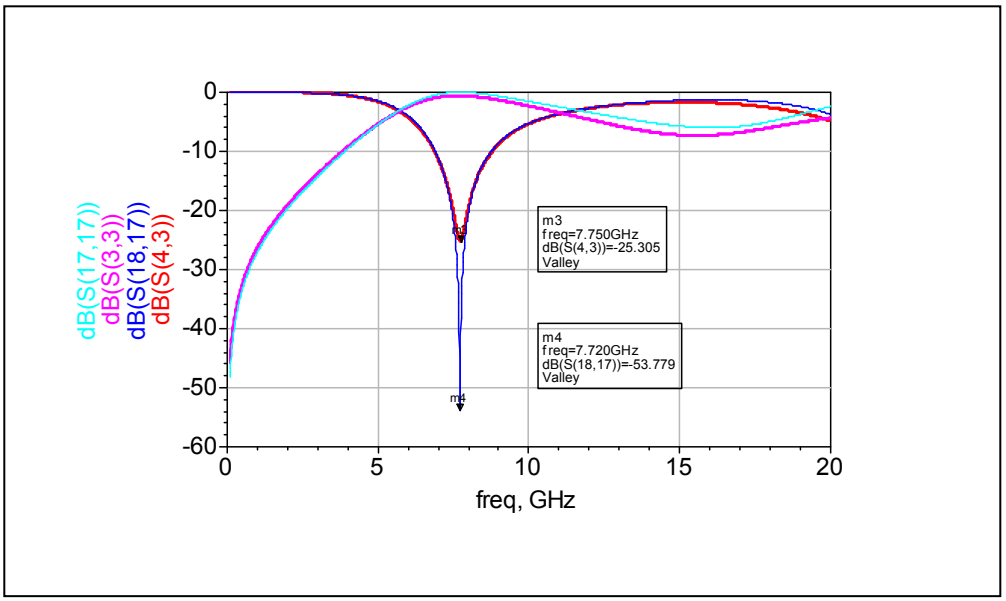



**Figure 17 Comparison of insertion and return loss HFSS vs circuit model. Oval anti-pad; Dk = 1; Anti-pad = 0.053”x0.055”**

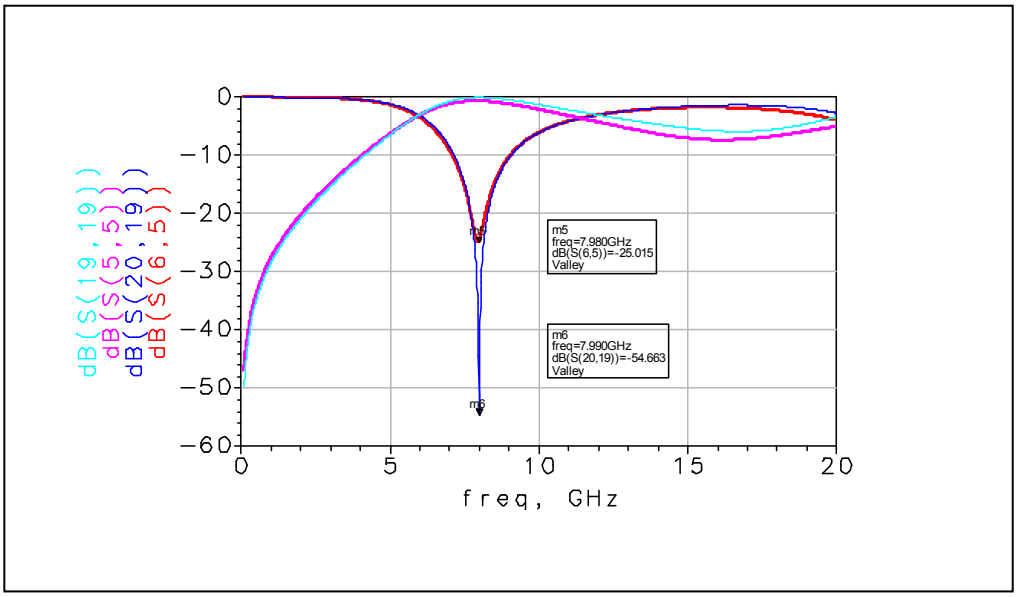



**Figure 18 Comparison of insertion and return loss HFSS vs circuit model. Oval anti-pad; Dk = 1; Anti-pad = 0.053”x0.060”**

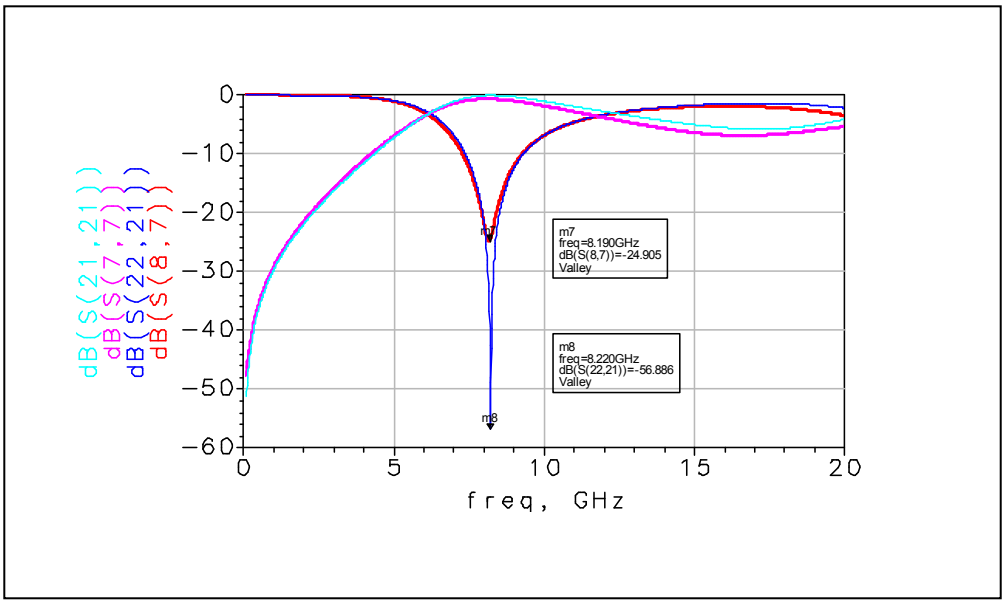



**Figure 19 Comparison of insertion and return loss HFSS vs circuit model. Oval anti-pad; Dk = 1; Anti-pad = 0.053”x0.065”**

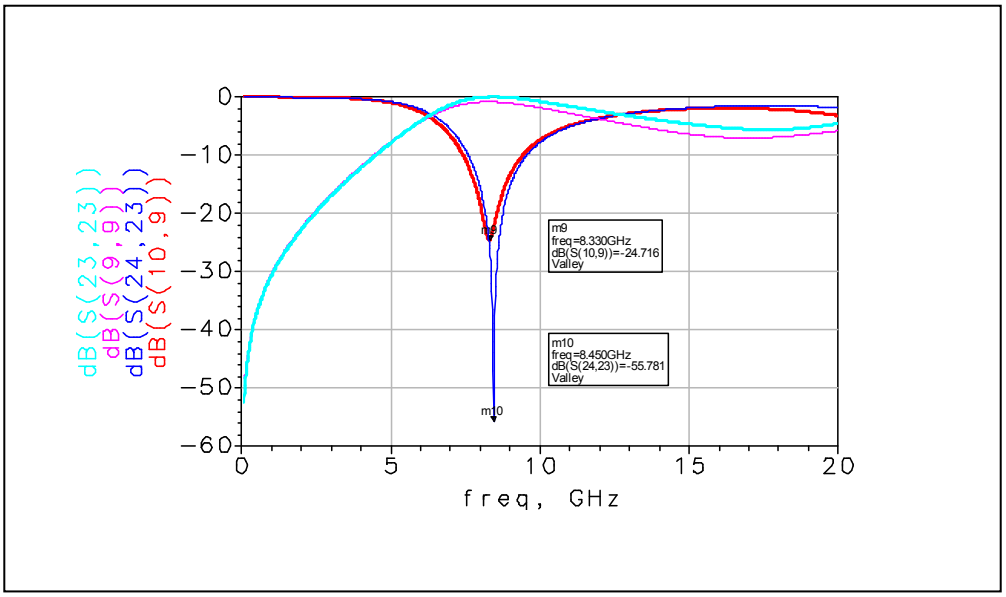



**Figure 20 Comparison of insertion and return loss HFSS vs circuit model. Oval anti-pad; Dk = 1; Anti-pad = 0.053”x0.070”**

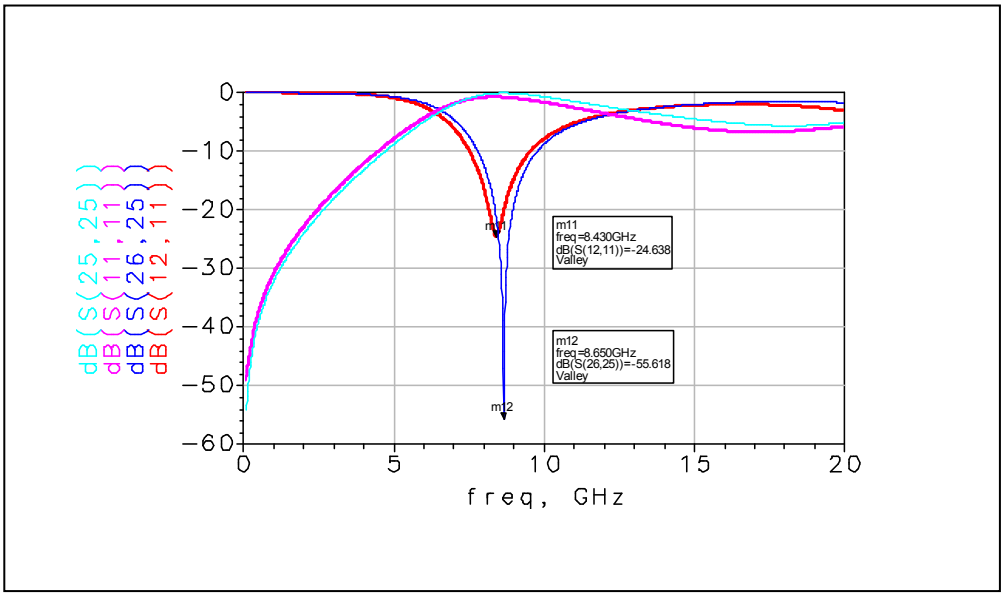



**Figure 21 Comparison of insertion and return loss HFSS vs circuit model. Oval anti-pad; Dk = 1; Anti-pad = 0.053”x0.075”**

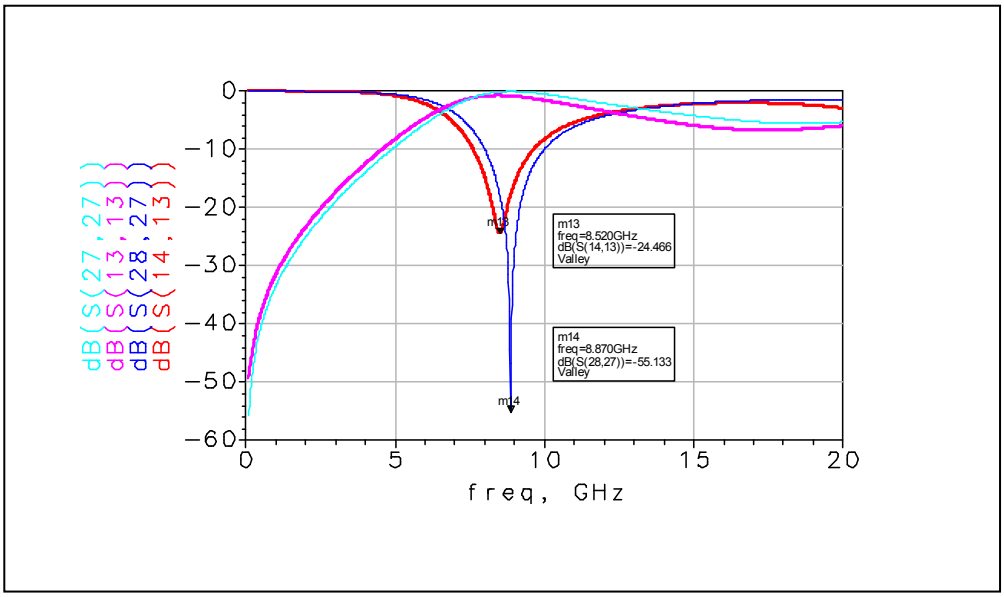



**Figure 22 Comparison of insertion and return loss HFSS vs circuit model. Oval anti-pad; Dk = 1; Anti-pad = 0.053"x0.080"**

**Table 3 Quarter-wave resonant frequency comparison summary**

| fo HFSS-GHz | fo Calc-GHz | Delta |
|---|---|---|
| 7.63 | 7.61 | -0.3% |
| 7.75 | 7.72 | -0.4% |
| 7.98 | 7.99 | 0.1% |
| 8.19 | 8.22 | 0.4% |
| 8.33 | 8.45 | 1.4% |
| 8.43 | 8.65 | 2.6% |
| 8.52 | 8.87 | 4.1% |

# Investigating the Stub Portion of the Via

The stub portion of the differential via under study is illustrated in Figure 23. In the PCB stack-up, the reference plane layers have oval anti-pads, while the signal layers have copper plane-fill with round anti-pads. Throughout Stub1 thickness, the anti-pads alternate between round and oval. The Stub2 thickness represents the power plane layers with thinner dielectric between planes and thicker copper layers.

The red portion of the cross-section represents the electric field while the blue rings represent the magnetic field. The electric field lines through Stub1 will spread onto the cavities between reference planes to roughly the extent of the round anti-pad diameter as

shown except for the thickness of the oval anti-pad copper layers where the electric field will be contained to the oval dimension. To simplify further analysis, these layers will be subtracted from Stub1 overall thickness and added to Stub2 thickness because they will have the same properties as Stub2.

Since excess via capacitance of Stub1 will be lower than Stub2, it will increase the speed of propagation through this section. Therefore, Dkeff1 will be lower than Dkeff2.

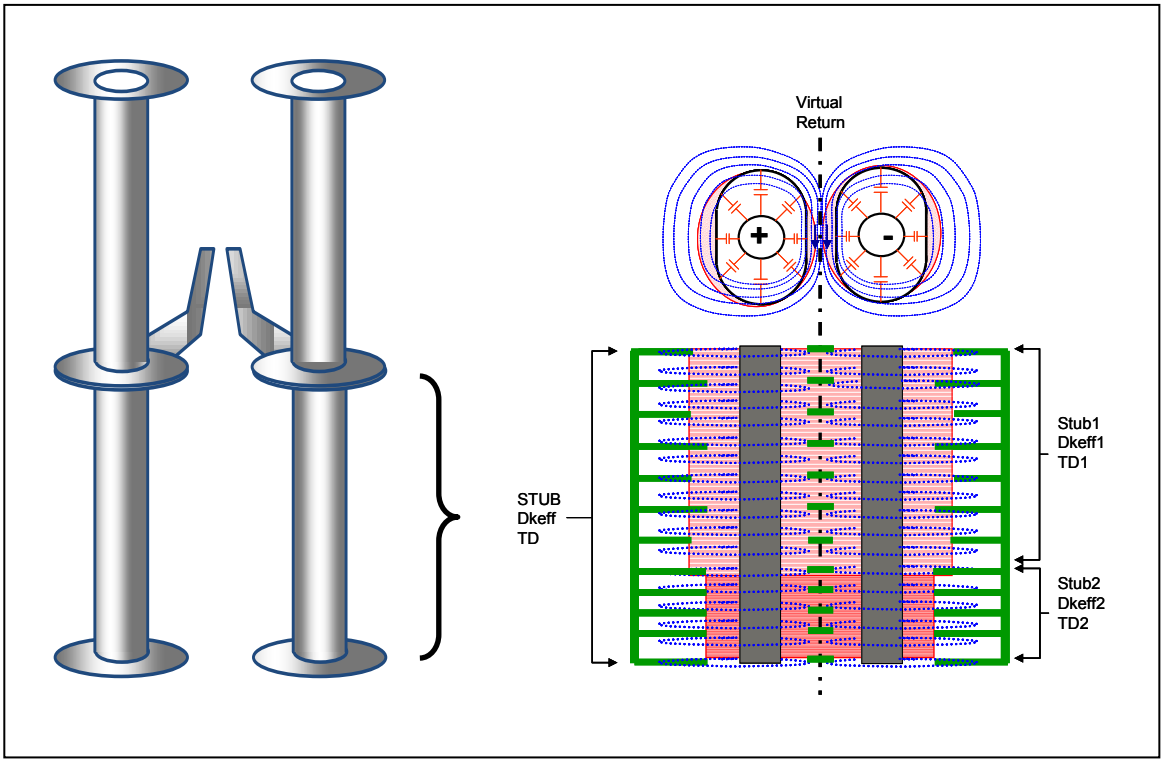



**Figure 23 Stub portion of differential via. Oval anti-pads on reference plane layers and round anti-pads on signal layers**

The relationship between stub length and resonant frequency using a sine wave example is illustrated in Figure 24. When a signal enters the via structure from the top, it travels along the through portion of the via until it reaches the junction of the internal track and stub. The signal splits with some of the signal continuing along the trace, and some continuing along the stub.

When the signal reaches the end of the stub, it reflects and travels back up the stub where it will again meet the attached signal trace. A portion will combine with the original signal and a portion will continue back toward the source. If the round trip delay 2TD is half a cycle, the two waves are 180 degrees out of phase, and the resulting amplitude at the receiver will be reduced.

The worst case for insertion loss is one half a wavelength delay. It occurs when the total delay through the stub, (*TD*) is ¼ wavelength. The frequency where this maximum cancellation occurs is called the ¼ wave resonant frequency *fo*.

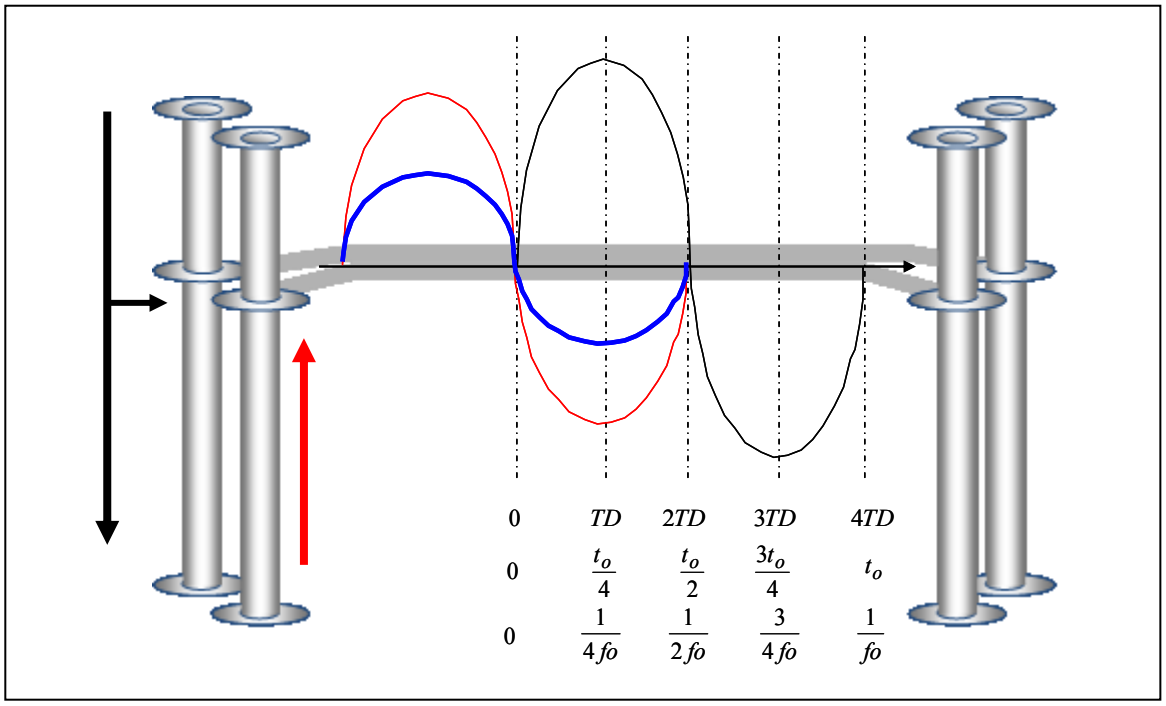
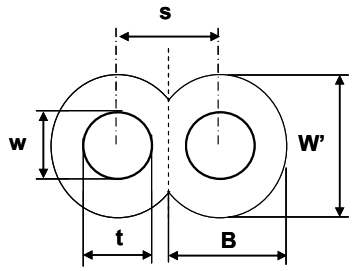
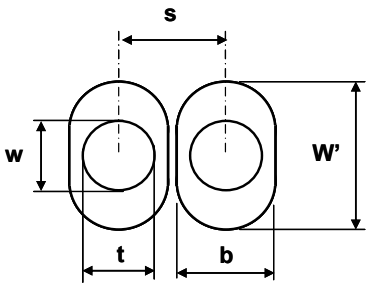



**Figure 24 Stub resonance illustration.**

The specifics of the differential via anti-pads are shown in Figure 25. The round anti-pads overlap each other due to the via-via spacing (*s*).




$$s = 0.059"$$
$$W' = 0.073"$$
$$B = \frac{s}{2} + \frac{W'}{2} = \frac{s + W'}{2} = \frac{0.059 + 0.073}{2} = 0.066"$$
$$w = t = 0.028"$$




$$s = 0.059"$$
$$W' = 0.073"$$
$$b = 0.053"$$
$$w = t = 0.028"$$

**Figure 25 Round vs. oval anti-pad details of the test vehicle.**

The propagation delay through the stub varies as the effective dielectric constant surrounding the via hole structure changes. The total time delay, TD is the sum of TD1 and TD2. A variation in signal speed due to variation in effective dielectric constant through the stub will determine the final ¼ wave frequency notch in the S21 insertion loss plot.

Therefore, the ¼ wave resonant frequency (Hz) can be expressed as;

$$fo = \frac{1}{4 \times TD} = \frac{1}{4 \times (TD_1 + TD_2)} = \frac{1}{4 \times \left( \frac{to_1}{4} + \frac{to_2}{4} \right)} = \frac{1}{(to_1 + to_2)}$$

$$fo = \frac{1}{\left[ \frac{1}{fo_1} + \frac{1}{fo_2} \right]} = \frac{fo_1 fo_2}{fo_1 + fo_2} \qquad \textbf{(18)}$$

Where;

$$fo_1 = \frac{1.18E+10}{4 \times Stub\_len1 \times l\sqrt{Dkeff1}} - Hz$$

$$fo_2 = \frac{1.18E+10}{4 \times Stub\_len2 \times \sqrt{Dkeff2}} - Hz$$

$$Dkeff1 = Dkavg \times \frac{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)}{\ln\left(\frac{W'+B}{w+t}\right)}$$

$$Dkeff2 = Dkavg \times \frac{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)}{\ln\left(\frac{W'+b}{w+t}\right)}$$

$s$ = via to via pitch – inches
$r$ = radius of via barrel = Drill dia. - inches
*Stub_len1; Stub_len2* = Stub length - inches

$$Dkavg = \frac{(Dkxy + Dkz)}{2}$$

$\left(\frac{W'+B}{w+t}\right)$ = Round anti-pad dimensions per Figure 25

$\left(\frac{W'+b}{w+t}\right)$ = Oval anti-pad dimensions per Figure 25

Once the ¼ wave resonant frequency is calculated, the new Dkeff and Zvia representing the entire stub length could be calculated using the following equations for each anti-pad dimension.

$$Dkeff = \left[\frac{1.18E+10}{4 \times Stub\_length \times fo}\right]^2$$

$$Zvia \cong \frac{(Zvia\_Stub1 + Zvia\_Stub2)}{2}$$

Where;

$$Zvia\_Stub1 \cong \frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+B}{w+t}\right)}$$

$$Zvia\_Stub2 \cong \frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+b}{w+t}\right)}$$

$s$ = via to via pitch - inches
$r$ = radius of via barrel = Drill dia. - inches
*Stub_len* =Stub length - inches

$$Dkavg = \frac{(Dkxy + Dkz)}{2}$$

## Circuit Model vs HFSS Via Model Validation

Using the HFFS model representing the actual test vehicle stack-up and long stub via pad/anti-pad stack, *Dkeff* and *Zvia* were calculated using the parameters listed below. The dielectric constants were provided from supplier's data sheet for the material used to fabricate the stack-up.

### HFSS Via Parameters;

$s$ = 0.059"
$r$ = Drill radius = 0.014"
*Via_length* = 14.7mil
*Stub_length1* = 212.9mils **
*Stub_length2* = 56.3mils **
*Stub_length* = 269.3mils
Anisotropy = 18%
*W'* = Anti-pad Length = 0.073"
$b$ = Oval anti-pad width = 0.053"
*B*= Round anti-pad width =0.066"
$w = t$ = Drill Diameter=0.028"

$Dk\_z = 3.65$

$Dk\_xy = 1.18 \times 3.65 \cong 4.3$

$$Dkavg = \left(\frac{3.65 + 4.3}{2}\right) = 3.96$$

***The combination of round anti-pad copper power planes and dielectric thickness for Stub1 defined by the HFSS test vehicle model is approximately 0.213". Subtracting this from total stub length of 0.269" leaves a length of approximately 0.056" for Stub1 (which includes the sum of the oval anti-pad copper thicknesses of Stub1 as explained earlier).*

### Circuit Model Calculated Via Parameters;

$$Dkeff1 = Dkavg \times \frac{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)}{\ln\left(\frac{W'+B}{w+t}\right)} = 3.96 \times \frac{\ln\left(\frac{0.059}{0.028} + \sqrt{\left(\frac{0.059}{0.028}\right)^2 - 1}\right)}{\ln\left(\frac{0.139}{0.056}\right)} = 6.00$$

$$Dkeff2 = Dkavg \times \frac{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right)}{\ln\left(\frac{W'+b}{w+t}\right)} = 3.96 \times \frac{\ln\left(\frac{0.059}{0.028} + \sqrt{\left(\frac{0.059}{0.028}\right)^2 - 1}\right)}{\ln\left(\frac{0.126}{0.056}\right)} = 6.73$$

$$fo_1 = \frac{1.18E+10}{4 \times Stub\_length1 \times \sqrt{Dkeff1}} = \frac{1.18E+10}{4 \times 0.2129 \times \sqrt{6.00}} = 5.66GHz$$

$$fo_2 = \frac{1.18E+10}{4 \times Stub\_length2 \times \sqrt{Dkeff2}} = \frac{1.18E+10}{4 \times 0.0563 \times \sqrt{6.73}} = 20.20GHz$$

$$fo = \frac{fo_1 \times fo_2}{fo_1 + fo_2} = \frac{5.66E+9 \times 2.02E+10}{5.66E+9 + 2.02E+10} = 4.42GHz$$

$$\boxed{Dkeff = \left[\frac{1.18E+10}{4 \times Stub\_length \times fo}\right]^2 = \left[\frac{1.18E+10}{4 \times 0.2693 \times 4.42E+9}\right]^2 = 6.15}$$

$$Zvia\_Stub1 \cong \frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+B}{w+t}\right)} = 33.7\Omega$$

$$Zvia\_Stub2 \cong \frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r} + \sqrt{\left(\frac{s}{2r}\right)^2 - 1}\right) \times \ln\left(\frac{W'+b}{w+t}\right)} = 31.8\Omega$$

$$\boxed{Zvia \cong \frac{(Zvia\_Stub1 + Zvia\_Stub2)}{2} = 32.8\Omega}$$

The simulated S-Parameters from the equivalent via circuit model was compared against the HFSS simulated touchstone s-parameter file using Agilent ADS [11]. Both circuit topologies used for the simulations are shown in Figure 26. Ideal Balun transformers were used to simplify the display of differential s-parameters.

Comparing the simulated insertion and return losses of Figure 27 shows excellent correlation between these two computation methods up to approximately 13GHz for such a simple model. It is also remarkable the ¼ resonant frequency calculated ($fo$ = 4.42GHz) agrees exactly to the simulated model.

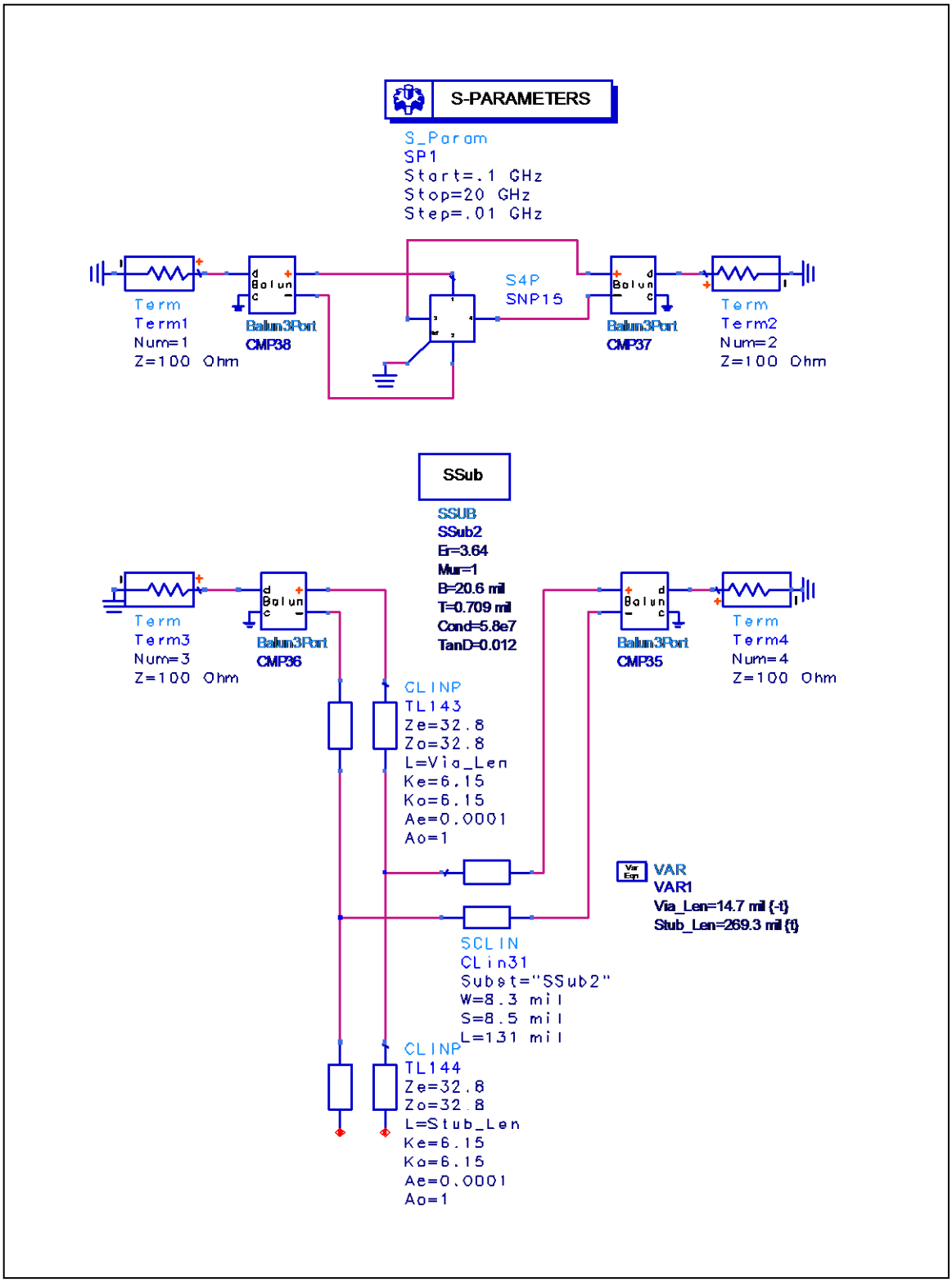



**Figure 26 ADS schematic of HFSS touchstone S-parameter file (*Dkxy* =4.3) vs. circuit model using calculated values.**

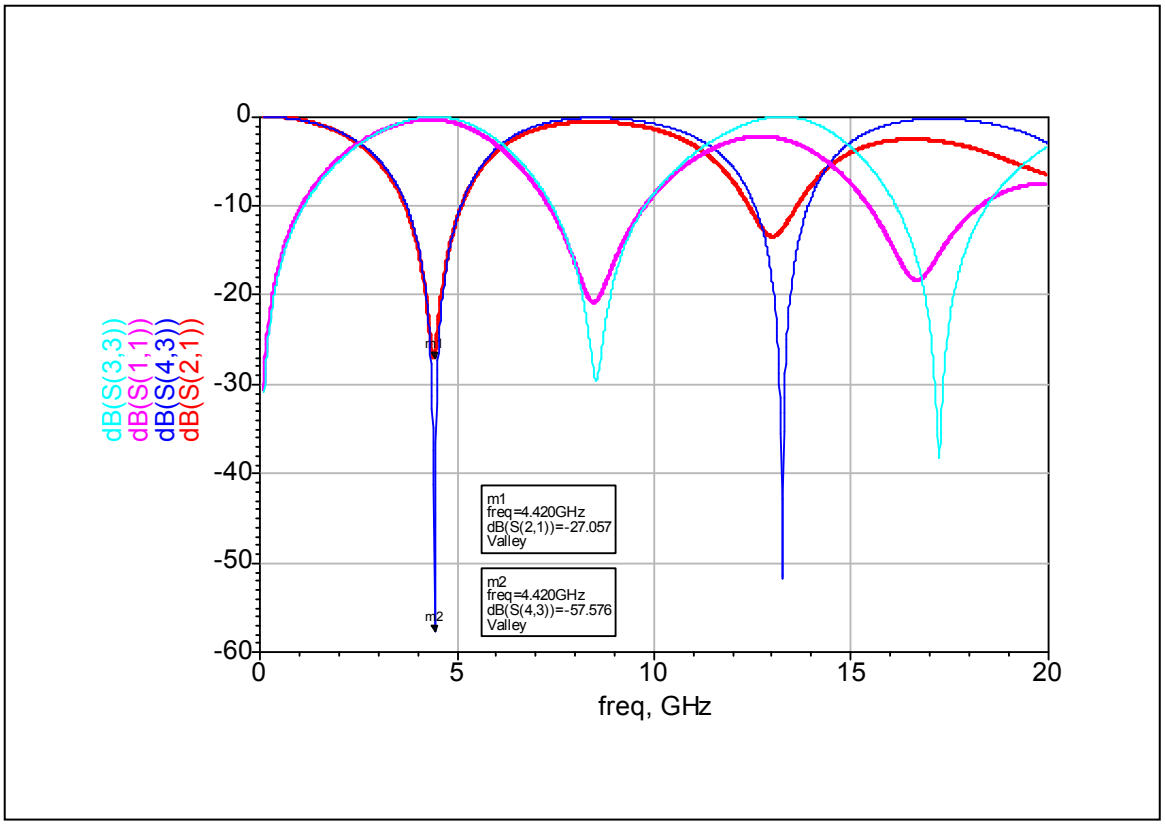



**Figure 27 Simulated insertion and return loss comparison of circuit model (blue, cyan) against HFSS simulation (red, magenta) respectively.**

## Circuit Model vs Test Vehicle Validation

Three sample via structures are illustrated in Figure 28. They represent a long, medium and short via stubs of the test vehicle and used to validate the transmission line circuit model accuracy.

The equivalent via circuit model for the long stub via case was compared against the HFSS generated touchstone s-parameter file and measured test vehicle results using Agilent ADS [11]. The test topologies used for the simulations are shown in Figure 29. The top circuit topology simulates the measured s-parameters of the test vehicle. The middle circuit topology simulates the HFSS s-parameter models for both vias and pcb traces. The bottom circuit topology tests the transmission line circuit models using analytical formula parameters for vias and traces. Ideal Balun transformers were used to simplify the display of differential s-parameters.

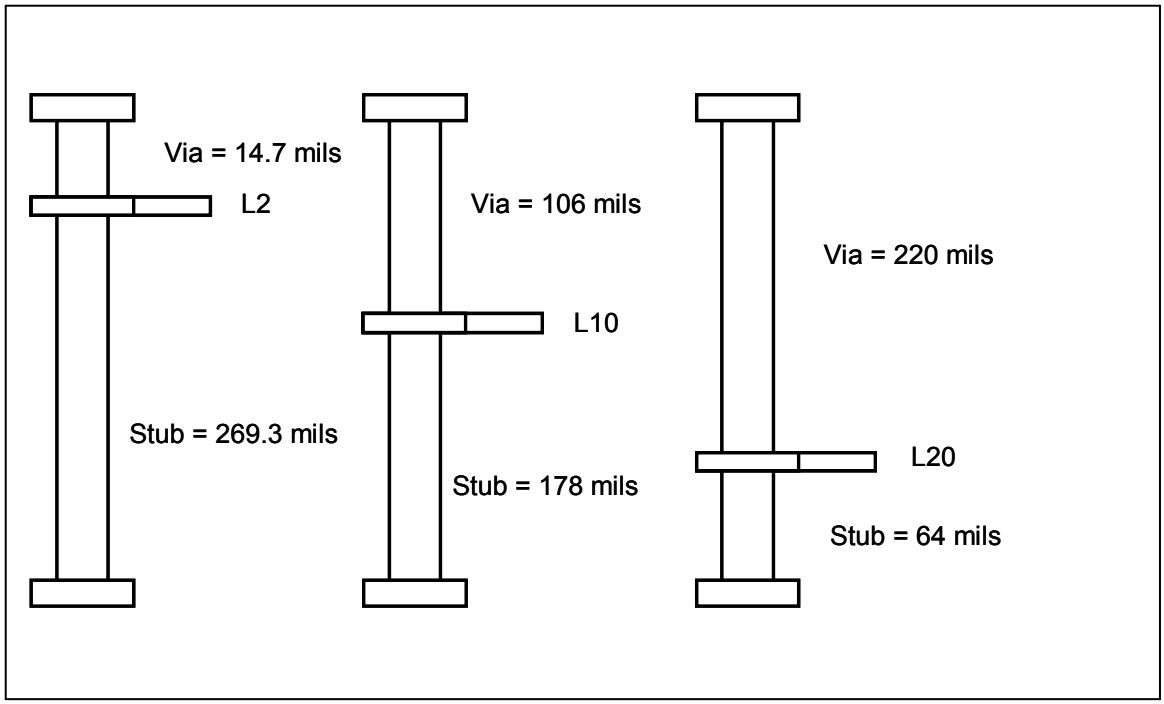



**Figure 28 Illustration of layers measured showing long, medium, short stub lengths from test vehicle stack-up.**

Figure 30 shows the correlation of calculated results used in the circuit model against the measured test vehicle structure and HFSS model of the long stub via. The calculated results for Dkeff = 6.15 and Zvia=32.8 Ω enables the model to be in excellent agreement with the measurements to about 13 GHz. It is a useful as a good first approximation to to perform what-if topology analysis or even provide a level of confidence the 3D models have been designed as expected.

Figure 31and Figure 32shows the correlation of calculated results used in the circuit model against the measured test vehicle for the medium and short stub vias respectively. Similarly, when Zvia = 32.8 Ω; *Dkeff* = 6.25 for medium stub and 6.57 for short stub, they show excellent agreement with measured results.

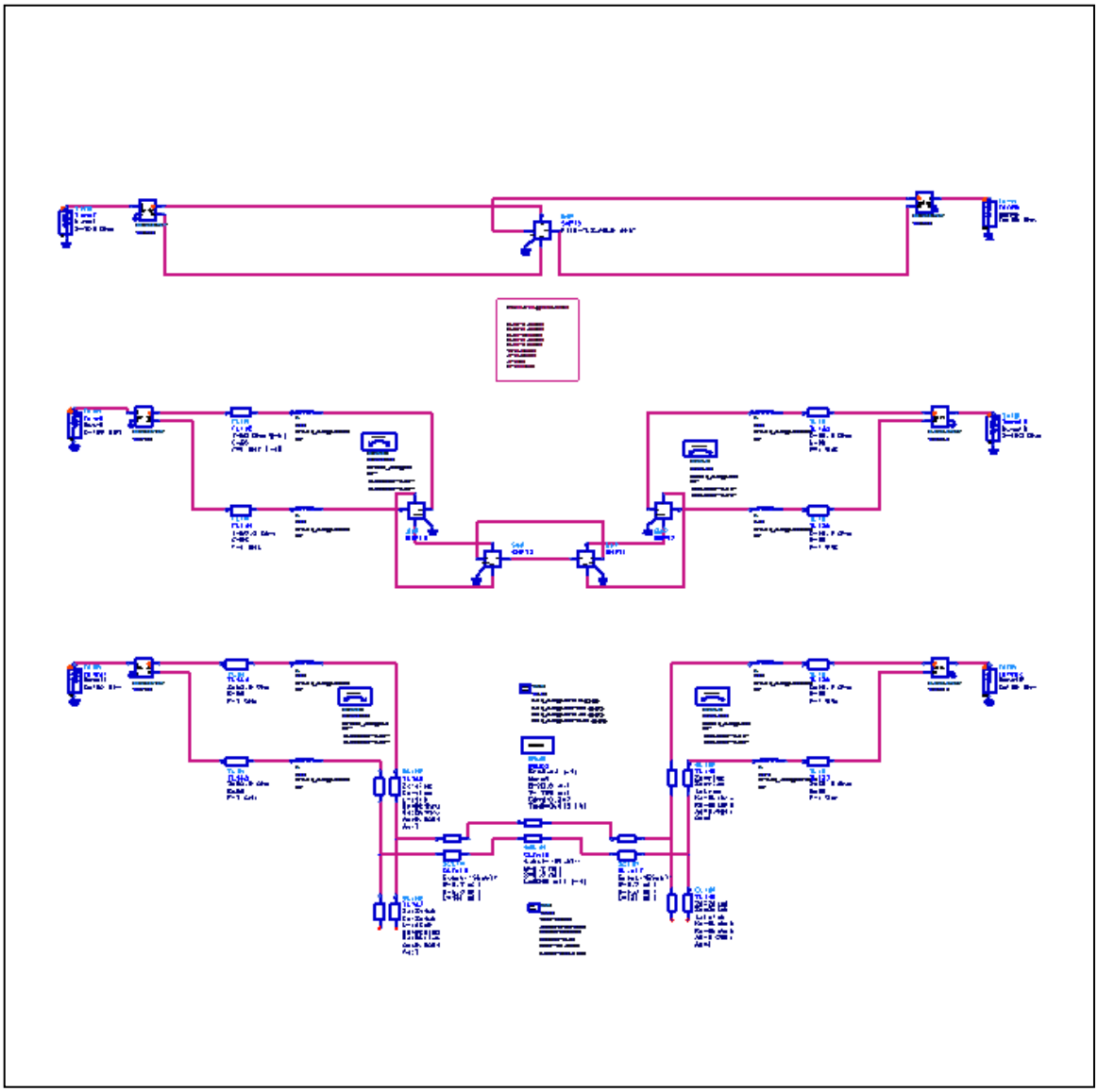


**Figure 29 ADS schematic of test vehicle (top), HFSS (middle) and circuit model (bottom) used for simulation comparisons. The HFSS topology includes both via and track s-parameter modeled from [7].**

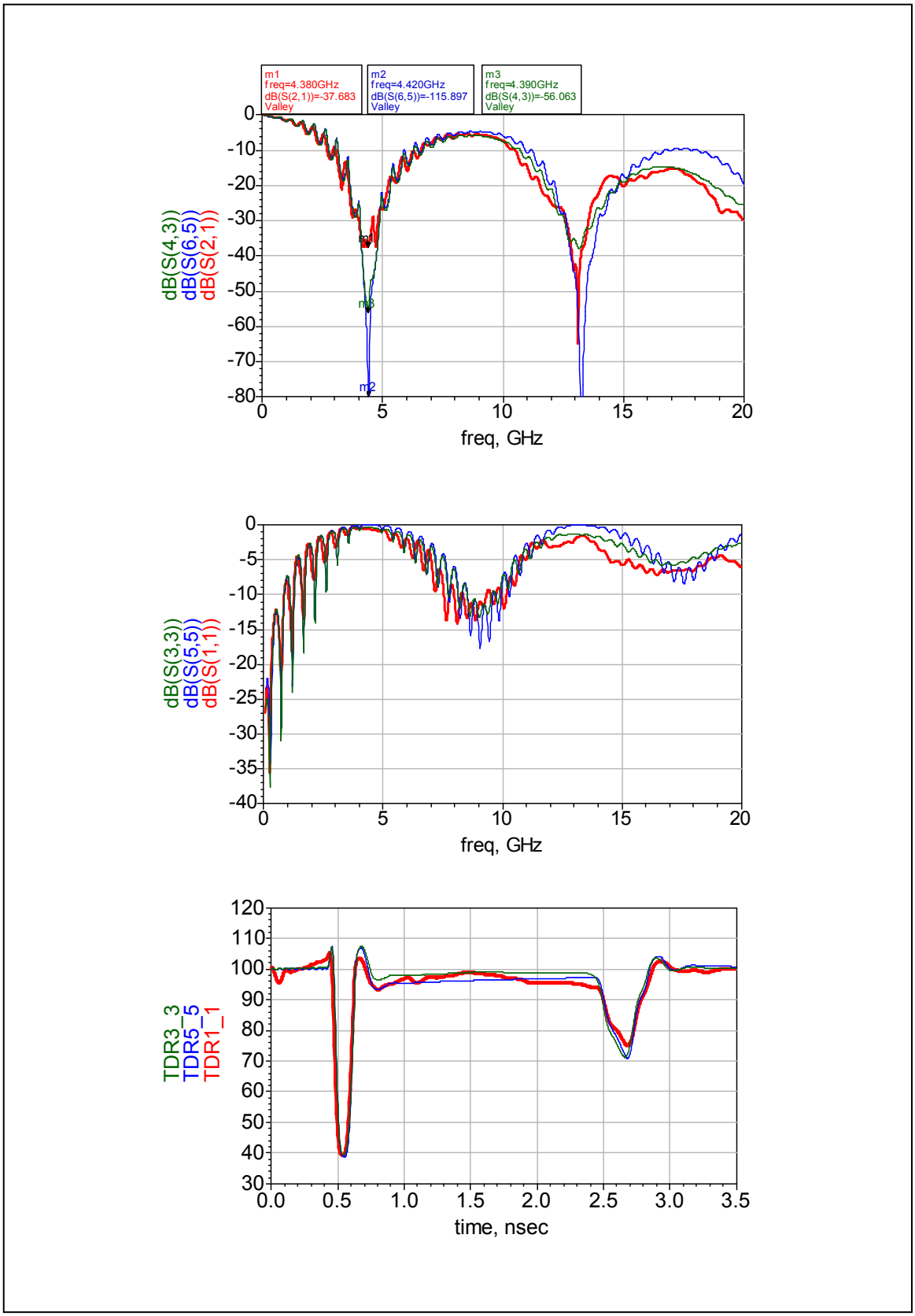



**Figure 30 Long stub (L2) via's insertion, return loss and TDR plots comparison of circuit model (blue) against HFSS simulation (green) and test vehicle measurements (red). Dkeff = 6.15, Zvia = 32.8, Df = 0.012.**

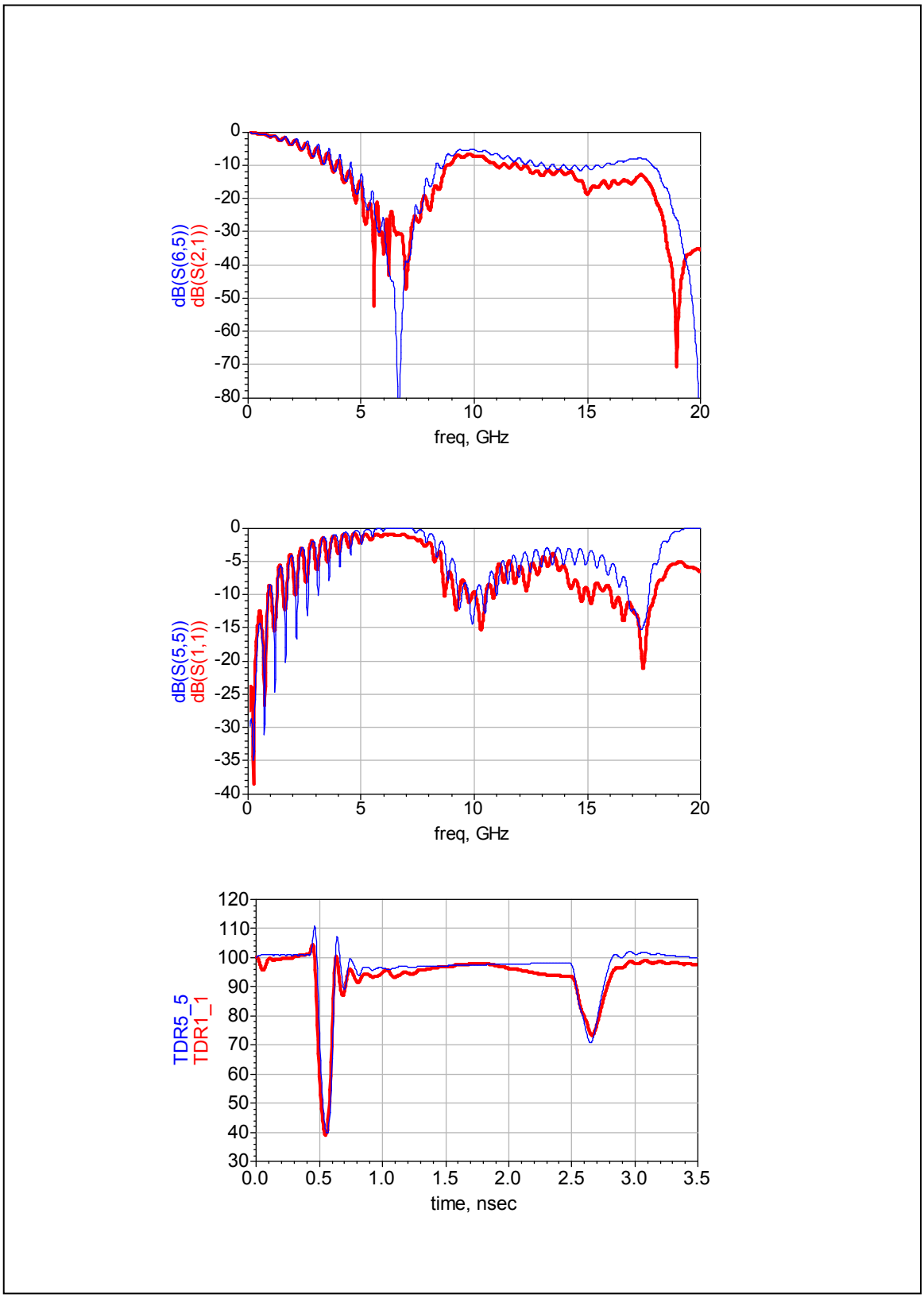



**Figure 31 Medium stub (L10) via's insertion, return loss and TDR plots comparison of circuit model (blue) against test vehicle measurements (red). Dkeff = 6.25, Zvia = 32.8, Df = 0.012.**

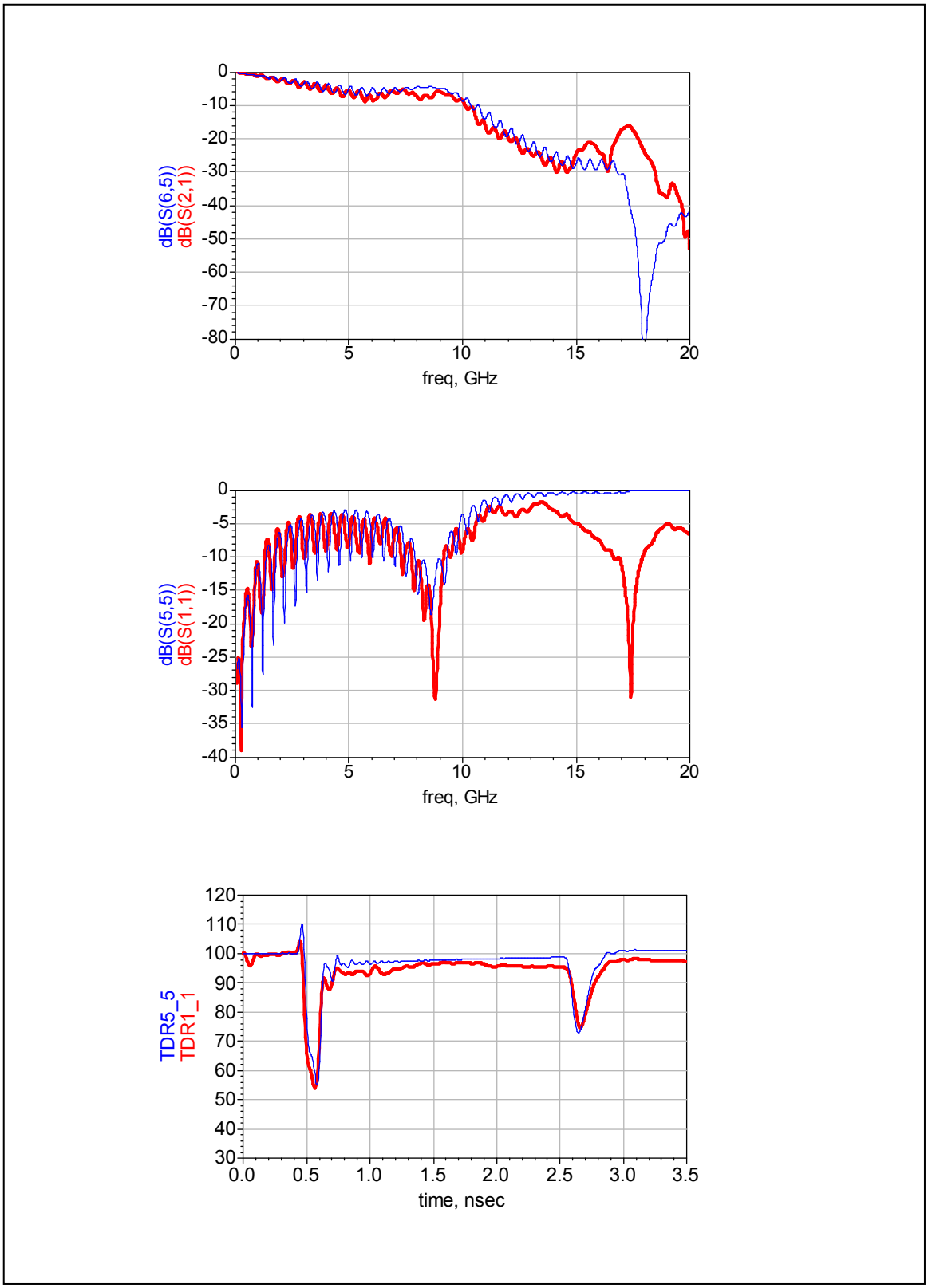



**Figure 32 Short stub (L20) via's insertion, return loss and TDR plots comparison of circuit model (blue) against test vehicle measurements (red). Dkeff = 6.57, Zvia = 32.8, Df = 0.012.**

# Conclusions

This work suggests a really simple circuit model for a differential via transition, consisting of two simple, coupled transmission line circuit models, can be used to accurately describe a real differential via to very high bandwidth.

The simple rod over plane formula can be used to predict the odd-mode inductance. The elliptical coaxial formula from [8] can be used to predict via capacitance due to anti-pad size to within 2% when compared against a 2D field solver [9].

This work has answered many of the questions from original papers [3] , [5] & [7]. Due to the anisotropic nature of the dielectric material, the effective dielectric constant in the x-y axis is typically higher than the dielectric constant in the z axis. This study revealed the dielectric material had an anisotropic factor of 18% and corroborates work done by [4]. It was possible to quantify and distinguish between a higher dielectric constant and a distributed capacitive loading from coupling to the planes.

In the absence of measured data, applying this methodology has proved to be remarkably accurate as a first approximation for calculating via impedance and effective dielectric constant. The values can easily be adjusted in the circuit model to quickly quantify the effects of adjusting various parameters for sensitivity analysis or to optimize the performance of vias in a channel model and to help sanitize subsequent models generated with a 3D EM-field solver. Using the developed formulae, a value of Dkeff = 6.15 and Zvia=32.8 Ω were found to be in excellent agreement with the measurements up to about 13 GHz.

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