A Broadband and Parametric Model of Differential Via Holes Using Space-Mapping Neural Network

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***Abstract*—This letter presents a novel broadband and completely parametric model of differential via holes by virtue of the space-mapping neural network technique. This model consists of a neural network and an equivalent circuit that is utilized to account for various EM effects of differential via holes. The neural network is trained to learn the multi-dimensional mapping between the geometrical variables and the values of independent circuit elements in the equivalent circuit. Once trained with the EM data, this model provides accurate and fast prediction of the EM behavior of differential via holes with geometry parameters as variables. Experiments in comparison with measurement data and EM simulations are included to demonstrate the merits of this new model in both the frequency and time domains.**

***Index Terms*—Differential via holes, parametric modeling, neural networks, space mapping.**

I. Introduction

WITH the continuous increase of clock frequency and layout density of high-speed circuits, differential via holes on multilayered printed circuit board have an important effect on signal quality issues such as bit error rate, crosstalk, reflections, or ground bounce. The design optimization of differential via holes often requires repetitive adjustments of the geometrical parameters. However, lack of fast, accurate, and parametric models becomes one of the design bottlenecks. Various modeling approaches have been reported [1]-[3]. Popular EM-field numerical simulations have been used for accurately solving the modeling problems. But the EM numerical approaches are time-consuming when the values of geometrical parameters vary repetitively. A characterization method was developed to model differential via holes as a cascade of capacitances and inductances [1]. This method required a special extraction process to calculate the values of capacitances and inductances at each designated location on via holes. A further time-domain macro-π model demonstrated a promising improvement in broadband accuracy [2]. The circuit elements in this macro-π model were expressed in terms of port-parameters instead of the actual geometrical variables. A partly parametric model based on the equivalent circuit extraction technique was developed to improve the accuracy over a broad bandwidth [3]. However, this advanced model has a complicated circuit topology with a large number of circuit elements, which leads to difficulty in parameter extraction and fitting. All these existing models are geometrically fixed. When the geometrical parameters of differential via holes are changed, the model needs to be re-developed.

This letter presents a novel broadband and completely parametric model of differential via holes on the multilayered printed circuit board by virtue of the space-mapping neural network (SMNN) technique. This new model exploits the merits of space-mapping technology [4]. It consists of an equivalent circuit and a neural network. The equivalent circuit is utilized to account for various EM effects of differential via holes. The widely used 3-layer neural network is trained to learn the multi-dimensional mapping between the geometrical variables and the values of independent circuit elements in the equivalent circuit. Once trained with the EM data, the proposed SMNN model preserves almost the same accuracy as EM simulations, yet works with the same computational speed as equivalent circuits. This parametric model is SPICE-compatible and can be readily used for geometry optimization of differential via holes in both the frequency and time domains.

II. Space-Mapping Neural Network Model

A. Equivalent Circuit for Differential Via Holes

The physical layout of differential via holes on multilayered printed circuit board is shown in Fig. 1. It is a four-port passive component, which is representative of a 26 layer design with 10 stripline layers used for differential pair routing. All reference layers are connected by two ground vias per differential pair vias. Each pair of via holes is connected through a coupled stripline with fixed line width of 0.203 mm, space of 0.229 mm, and length of 152.4 mm. The space between each intra-pair via is 1.499 mm and the adjacent ground via is 2.007 mm away for each respective signal via. The layout is embedded into a dielectric material N4000-13^{TM}. The total dielectric spacing between the reference planes is nominally 0.551 mm. The thicknesses of core and prepreg materials are 0.254 mm and 0.279 mm, respectively. The metallic layers are copper with thicknesses of 0.5 ounce and conductivity values of 5.8×10^7 Siemens/m. Considering the EM simulation time and memory requirement of this complicated and large structure, the entire geometrical structure was segmented into four parts: two Segment 1 (for the two couples of differential via holes) and two Segment 2 (for the coupled striplines) each with line length of 76.2 mm as shown in Fig.1 (b). S-parameters of each segment were obtained separately through HFSS EM simulations [5] and then these S-parameters are combined to produce the overall

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EM responses.

Fig. 2 shows the equivalent circuit for differential via holes on the multilayered printed circuit board. In this equivalent circuit, the differential via hole was modeled as two separated lossy coupled transmission line models (i.e., CLINP 1 and 2) in ADS [6] where one part is the via portion of the signal path from outer layer to a particular inner signal layer. The other part is the stub portion. All these via segments and stubs used the same values of effective dielectric constant (D_k) and odd mode impedance (Z_o) for respective layer topology model. An edge-coupled stripline (SCLIN) model in ADS was used to represent the 6 inches coupled stripline. C_m models the mutual capacitance between the two pads on the top layer. C_1 represents the capacitive coupling between the pad and the reference ground plane. C_2 models the capacitance between the via holes and the reference ground planes. Open-circuited stubs are used to model the open-circuited effect of via stubs.

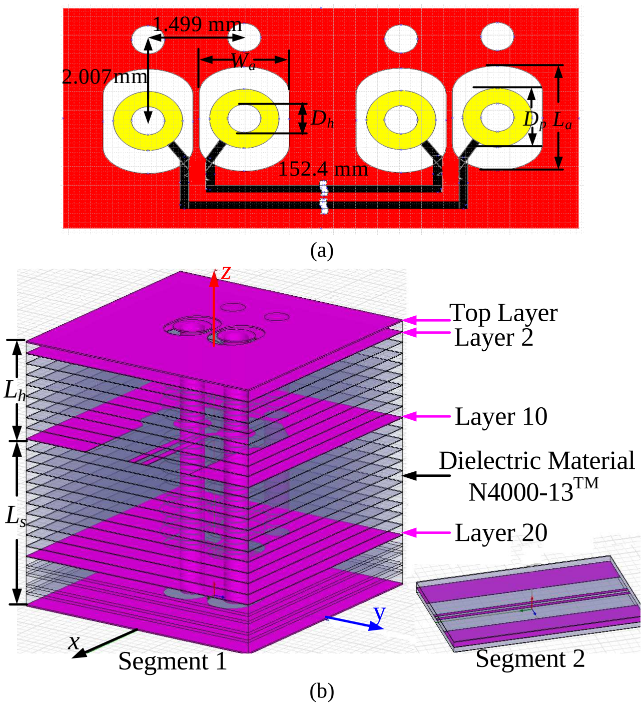

Fig.1. (a) Top view of the layout of differential via holes on multilayered printed circuit board, (b) Entire structure is segmented into two Segment 1 (for the two couples of differential via holes) and two Segment 2 (for the coupled striplines) each with line length of 76.2 mm (half of total length).

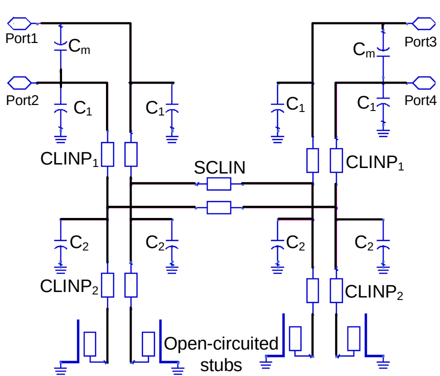

Fig. 2. Equivalent circuit for differential via holes.

B. Structure of the Proposed SMNN Model

The structure of proposed SMNN model is illustrated in Fig. 3. It consists of a neural network and an equivalent circuit. Let $\boldsymbol{x}$ represent the inputs of the neural network defined as six geometrical variables of differential via holes, i.e. diameter of via holes (D_h), diameter of pads (D_p), width of anti-pads (W_a), length of anti-pads (L_a), length of via holes (L_h) and length of stubs (L_s) as illustrated in Fig. 1. Let $\boldsymbol{C_e}$ represent the outputs of the neural network specified as five independent circuit elements in the equivalent circuit, i.e., effective dielectric constant (D_k), odd mode impedance (Z_o) of CLINP models, C_m, C_1 and C_2 as illustrated in Fig. 2. The neural network is trained to learn the multi-dimensional mapping between $\boldsymbol{x}$ and $\boldsymbol{C_e}$. Let $\boldsymbol{d}$ represent the outputs of EM simulations, i.e., magnitudes and radians of differential S-parameters SDD11 and SDD21. Let $\boldsymbol{y}$ represent the outputs of the equivalent circuit. The objective here is to adjust the neural network internal weights such that the mean square error between the available training data $\boldsymbol{d}$ and $\boldsymbol{y}$ is minimized

$$E(\boldsymbol{w}) = \frac{1}{2n}\sum_{k=1}^{n}\sum_{j=1}^{F_p}\left\| \boldsymbol{y}\left(\boldsymbol{P}\left(\boldsymbol{w},\boldsymbol{x}_k\right), freq_j\right) - \boldsymbol{d}\left(\boldsymbol{x}_k, freq_j\right)\right\|^2 \quad (1)$$

where $\boldsymbol{w}$ denotes the internal weights of the neural network, n is the total number of training geometry samples, F_p is the number of frequency points, and $\boldsymbol{P}$ represents the mapping between $\boldsymbol{x}_k$ and $\boldsymbol{C}_e$ through the neural network

$$\boldsymbol{C}_e = \boldsymbol{P}\left(\boldsymbol{w},\boldsymbol{x}_k\right) \quad (2)$$

This process is accomplished using the quasi-Newton algorithm in *NeuroModeler* [7]. Once trained with the EM data, the SMNN model for differential via holes is established.

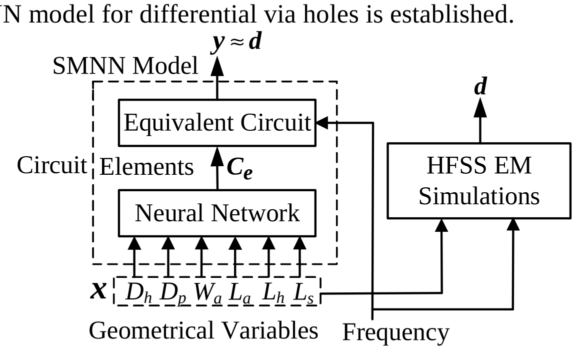

Fig.3. Structure of the proposed SMNN model for differential via holes.

III. Experiments and Results

The SMNN technique is applied to the broadband and parametric modeling of the differential via holes on the multilayered printed circuit board. There are 360 sets of training data as defined in Table I. Partial composite design of experiments method [8] is used to determine the distribution of training data samples. The lengths of via holes (L_h) and stubs (L_s) are determined by the position of signal layer within the board stack-up. Three different via stubs representing long, medium and short stubs for layers 2, 10 and 20, respectively, are performed in our study. Because most reinforced laminates with layers of woven glass had dielectric anisotropy of 15-20% [9], our investigations show that the transverse dielectric constant $D_k(z)$ of 3.58 and 3.69 (from ParcNelco dielectric calculator for the respective cores and prepregs materials) and a longitudinal dielectric constant $D_k(x/y)$ of average value 4.3 in HFSS EM simulations produce the best match with the quarter wave frequency notch of measurement data. The frequency range of interest is from DC to 20 GHz with step size of 0.1 GHz.

Fig. 4 depicts the frequency-domain differential responses of SDD21 and the time-domain differential responses of TDD11 by the proposed SMNN model for three different geometries #1, #2, and #3, which are never used during the training, in comparison with EM simulations and measurement data. The geometrical parameters of three differential via holes are as follows: D_h =0.711 mm, D_p= 1.092 mm, W_a = 1.346 mm, L_a= 1.854 mm for layer 2 (#1), layer 10 (#2), layer 20 (#3) as shown in Fig. 1. The time-domain differential responses are derived using a time- domain reflector function from the S-parameter data within ADS. The S-parameter measurements were performed on these three differential via holes using Agilent NS230A, 4 port 20GHz Vector Network Analyzer. The 3-layer neural network with 20 neurons in the hidden layer was constructed in our model. Broadband accuracy of the proposed model is confirmed by its good agreement with the EM simulations and measurement data in both the frequency and time domains. A relatively lower accuracy at high frequency is because that this model did not include the parasitic probe fixture effects which are part of the device under measurement, nor did it consider a higher value for dissipation factor for the dielectric which is often the case. Our proposed SMNN model correctly predicts the quarter wave resonant frequency at 4.3 GHz and 6.3 GHz which match the measurement data for two different geometries #1 and #2, respectively.

The advantage of using the proposed SMNN model is also realized in terms of CPU time compared to EM simulations. The evaluation of three different geometries #1, #2, and #3 takes only 2.75s by the proposed SMNN model in sharply contrast to 10.2 hours by the HFSS EM simulations.

TABLE I. Definition of Training Data

Parameters	Training data (360 sets)		
	Min	Max	Step
D_h (mm)	0.508	0.762	0.0508
D_p (mm)	0.889	1.143	0.0508
W_a (mm)	1.143	1.905	0.127
L_a (mm)	1.321	2.032	0.1016
Layer 2: L_h = 0.356 mm L_s =6.858 mm; Layer 10: L_h =2.692 mm L_s =4.521 mm; Layer 20: L_h =5.588 mm L_s =1.626 mm.			

IV. Conclusion

A broadband and completely parametric model of differential via holes on multilayered printed circuit board using the SMNN technique has been introduced. Instead of applying the stiff and time-consuming parameter fitting by human, this model utilizes the neural network to learn the mapping between the geometrical variables and the values of independent circuit elements in the equivalent circuit through an automated training process. Once trained, the proposed SMNN model provides accurate and fast prediction of the EM behavior of differential via holes and can be used in high-level simulation and optimization with geometrical parameters as design variables.

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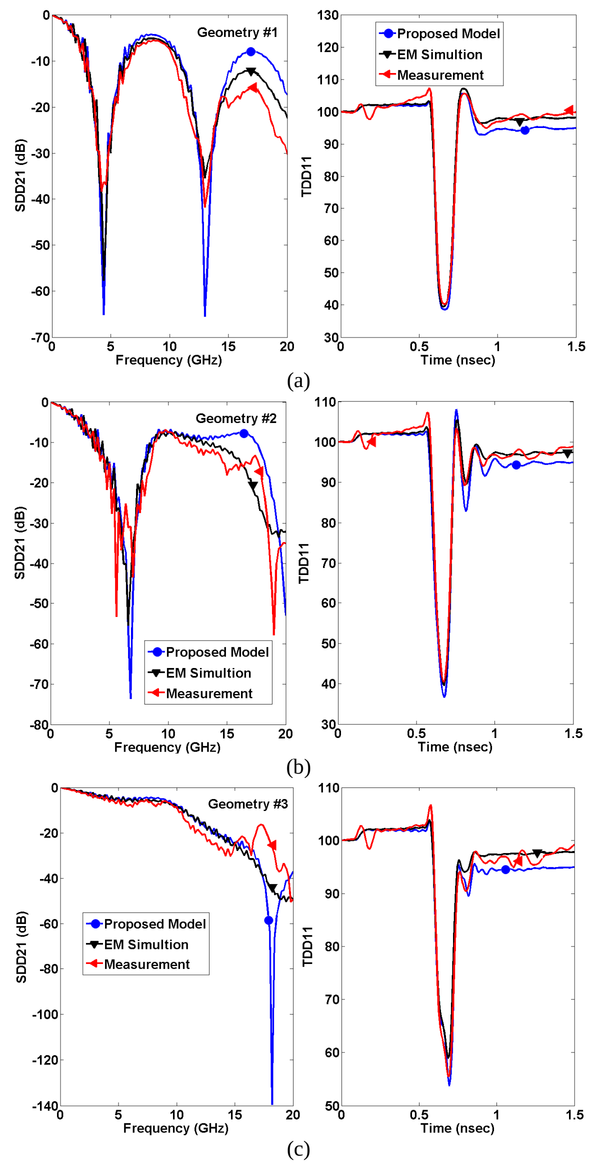

Fig.4. Comparison of frequency-domain responses of SDD21 and time-domain responses of TDD11 by the proposed SMNN model, EM simulations and measurement data for three different geometries #1(a), #2(b), and #3(c).