Guard Traces

White Paper-Issue 02

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Abstract:

To guard or not to guard? That is the question often asked by digital hardware design engineers. As bit rates continue to climb, there is increased debate on whether to use guard traces to control crosstalk in high-speed digital signaling. By doing so, it is believed the guard trace will act as a shield between the aggressor and victim traces. On the other hand, the argument is that merely separating the victim trace to at least three times the line width from the aggressor is good enough. This paper studies the application of guard traces and quantifies the results against non guarded scenarios.

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1. Issue Draft: May 21, 2012; Initial draft release.
2. Issue 01: May 24, 2012 Final Release.
3. Issue 02: May 28, 2012 Follow-up studying effect of dielectric height in Microstrip geometry.

GUARD TRACES

Introduction:

As bit rates continue to climb, there is increased debate on whether to use guard traces to control crosstalk in high-speed digital signaling. By definition, a guard trace is a trace routed coplanar between an aggressor line and a victim line. Often the guard trace is terminated at each end in its characteristic impedance or shorted to ground. To be most effective, the guard trace should be shorted to ground at regular intervals along its length using stitching vias spaced at 1/10th of a wavelength of the highest frequency component of the aggressor's signal. By doing so, it is believed the guard trace will act as a shield between the aggressor and victim traces.

On the other side of the debate, the argument is that merely separating the victim trace to at least three times the line width from the aggressor is good enough. The reasoning here is that crosstalk falls off rapidly with increased spacing anyways, and by adding a guard trace, you will already have at least three times the trace separation to fit it in. Furthermore, the added ground stitching will severely restrict routing of other signals on the board. Of course the only way to settle these kinds of debates is to put in the numbers.

In order to answer the question, "To guard or not to guard?", this white paper studies the effect of applying guard traces, and quantifies the results against the non guarded scenario.

Discussion

When two coplanar parallel traces running in close proximity, as shown in Figure 1, there are two types of crosstalk generated; Near-End (NEXT), or backwards crosstalk, and Far-End (FEXT), or forward crosstalk.

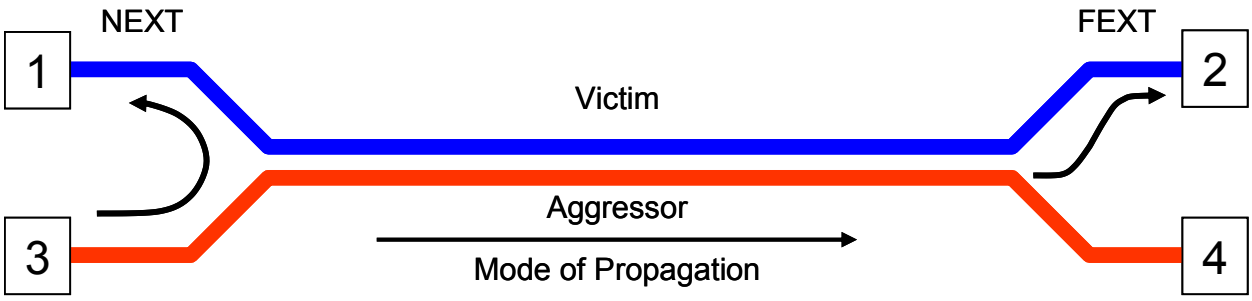

Figure 1 Illustration of NEXT and FEXT. As the aggressor signal propagates from port 3 to port 4, Near-End XTalk appears on port 1 and Far-End XTalk appears on port 2 after one Time Delay (TD) of the interconnect.

NEXT voltage is correlated to the coupled current through a terminating resistor (not shown) at port 1. The backward crosstalk coefficient, *Kb*, is equal to the ratio of *Vb/Va,* as defined by Equation 1; where *Vb* is the voltage at port 1; and *Va* is the peak voltage of the aggressor at port 3.

Equation 1

$$K_b = \frac{V_b}{V_a}$$

The general signature of the NEXT waveform, for a linear ramp aggressor, is shown in Figure 2. *Vb*, shown in blue, is the backward crosstalk voltage, while *Va*, shown in red, is the aggressor voltage. The backward crosstalk voltage continues to increase in response to the rising edge of the aggressor until it saturates after the aggressor's rise-time. The duration of NEXT waveform lasts for twice the time delay, TD of the topology.

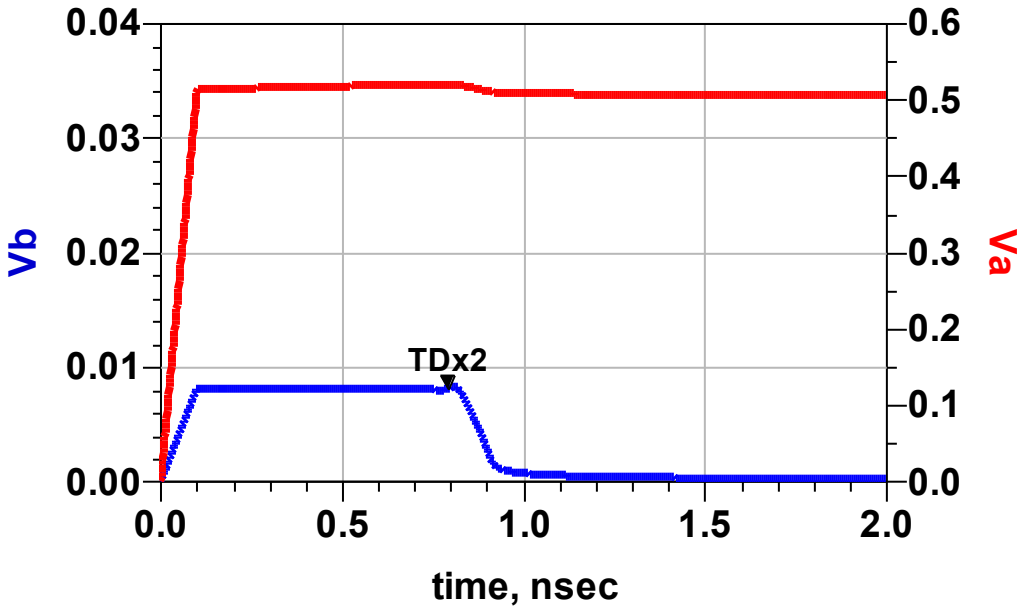

Figure 2 NEXT voltage signature, Vb (blue), is backward crosstalk voltage in response to a linear step aggressor voltage, Va (red). TDx2 is twice the time delay. Simulated with Agilent ADS

The magnitude of the NEXT voltage is a function of the coupled spacing between the two traces. As the two traces are brought closer together, the mutual capacitance and inductance increases and thus the NEXT voltage, *Vb*, will increase as defined by Equation 2 [1]:

Equation 2

$$V_b = K_b \times V_a = V_a \times \frac{1}{4}\left(\frac{Cm}{Co} + \frac{Lm}{Lo}\right)$$

Where:

Vb = NEXT voltage – V.

Va = Aggressor voltage – V.

Kb = NEXT coefficient.

Cm = Mutual capacitance per unit length in pF/inch.

Lm = Mutual inductance per unit length in nH/inch.

Co = Trace capacitance per unit length in pF/inch.

Lo = Trace inductance per unit length in nH/inch.

The only practical way to calculate *Kb* is to use a 2D field solver to get the inductive and capacitance matrix elements. Alternatively, if the field solver provides the coupled odd and even mode impedances, *Zodd* and *Zev*, then *Kb* can be calculated using Equation 3.

Equation 3

$$K_b = \frac{\sqrt{Z_{ev}} - \sqrt{Z_{odd}}}{\sqrt{Z_{ev}} + \sqrt{Z_{odd}}}$$

FEXT voltage is correlated to the coupled current through a terminating resistor (not shown) at port 2 of Figure 1. The forward crosstalk coefficient, *Kf*, is equal to the ratio of *Vf/Va,* as defined by Equation 4; where *Vf* is the voltage at port 1; and *Va* is the peak voltage of the aggressor.

Equation 4

$$K_f = \frac{V_f}{V_a}$$

The general signature of the FEXT waveform, for a linear ramp aggressor, is shown in Figure 3. *Vf*, shown in blue, is the forward crosstalk voltage at port 2; while *Va* , shown in red, is the aggressor voltage appearing at the far end port 4. FEXT voltage differs from NEXT in that it only appears as a pulse at TD after the signal is launched. In this example, the negative going FEXT pulse is the derivative of the aggressor's rising edge at TD. The opposite is true on the falling edge of an aggressor.

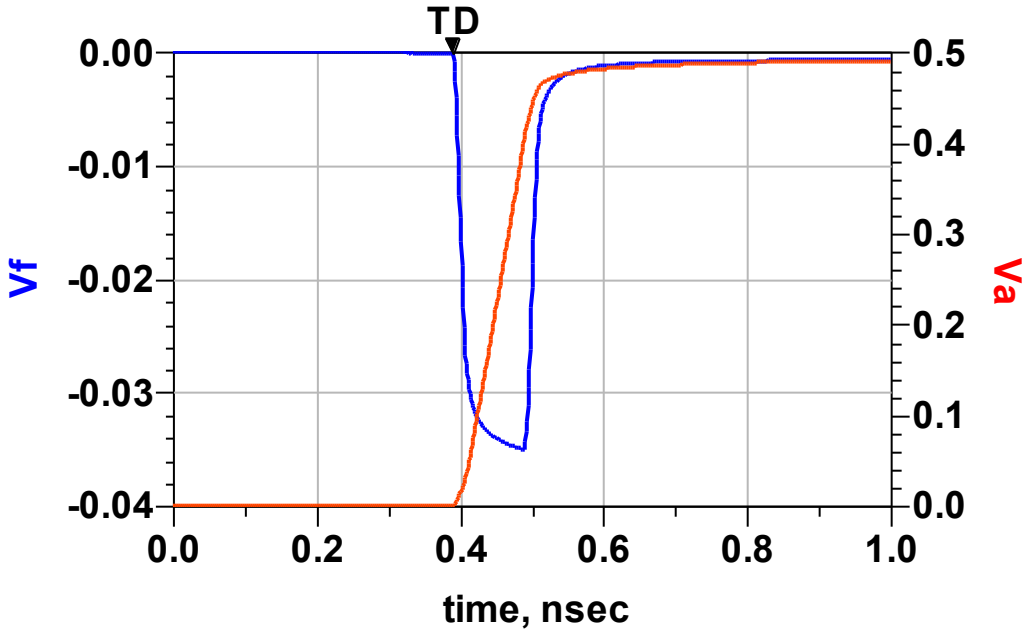

Figure 3 FEXT voltage signature, Vf (blue), is forward crosstalk voltage in response to a linear step aggressor voltage, Va (red). TD is the time delay (3 inches) to the far end. Simulated with Agilent ADS

Unlike the NEXT voltage, the peak value of FEXT voltage scales with the coupled length. It peaks when its amplitude grows to a level comparable to the voltage at 50% of the aggressor's risetime at TD as shown in Figure 4. In this example, the coupled lengths are: 3, 6, 10 and 15 inches respectively.

In the same way the aggressor waveform couples FEXT voltage onto the victim, FEXT couples noise back onto the aggressor affecting the risetime as shown. Due to superposition, the aggressor waveform shown at each TD is the sum of the FEXT voltage and the original transmitted waveform that would have appeared at TD with no coupling. A delay in the rising edge reduces the set-up and hold margins at the receiver as well as other timing issues if it happens to be a clock.

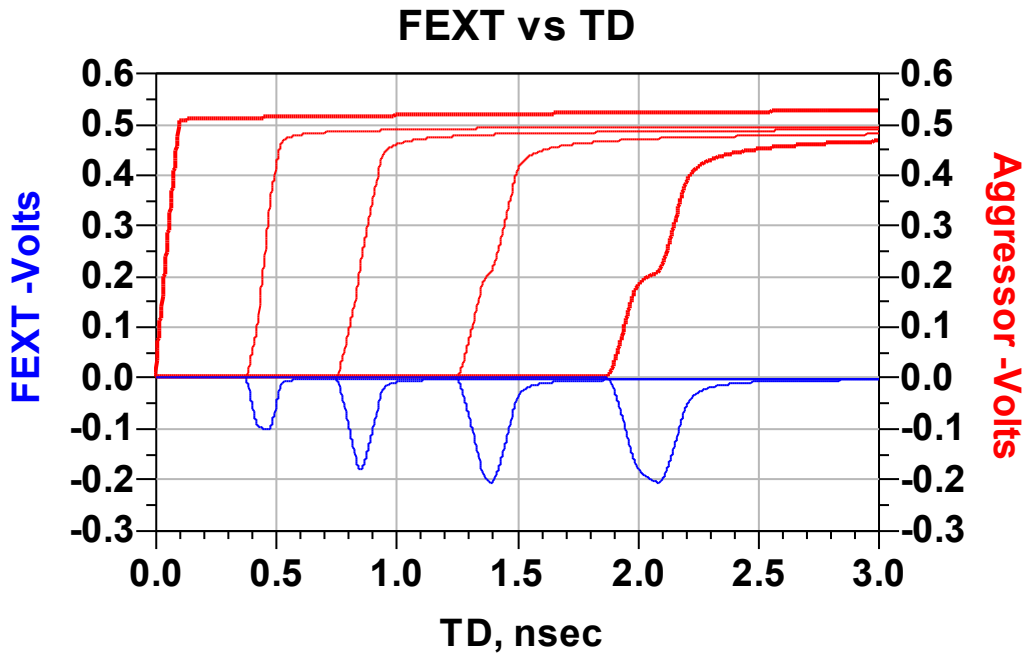

Figure 4 FEXT voltage increase vs TD for coupled lengths of 3, 6, 10 and 15 inches respectively. Microstrip geometry; 5 mil track, 5 mil space topology. Incident risetime is 100 psec. Simulated with Agilent ADS.

If the rise-time at TD is known, the FEXT voltage can be predicted by the following Equation 5[1]:

Equation 5

$$V_f = K_f \times V_a = \left[\frac{\sqrt{Dkeff} \times Len}{2 \times t_r \times c} \times \left(\frac{Cm}{Co} - \frac{Lm}{Lo}\right)\right] \times V_a$$

Where:

Vf = FEXT voltage – V

Va = Aggressor voltage -V

Kf = FEXT coefficient

Cm = Mutual capacitance per unit length in pF/inch

Lm = Mutual inductance per unit length in nH/inch.

Co = Trace capacitance per unit length in pF/inch.

Lo = Trace inductance per unit length in nH/inch.

t_r = Risetime (10-90%) of aggressor signal at TD in sec.

c = Speed of light – 1.18E10 inches/sec.

Dkeff = Effective permittivity or also known as effective dielectric constant surrounding the trace.

Len = Length of trace -inches.

Although the inductive and capacitive matrix elements can be obtained using a 2D field solver, the rise-time is more difficult to predict. This is because of risetime degradation due to skin effect and dielectric losses, as well as impedance variations along the line causing reflections. But worst of all, as seen in Figure 4, is the forward crosstalk coupling affecting the aggressor's risetime makes it next to impossible to predict. The only practical way to calculate *Kf* is to model and simulate the topology using a circuit simulator that supports coupled transmission lines. The circuit simulator should have an integrated 2D field solver built in to allow automatic generation of a coupled transmission line model from the cross-sectional information. As will be shown in later, one such tool that is perfect for this task is Agilent`s EEsof EDA Design Software (ADS).

In stripline geometry, generally speaking, there is only NEXT; while In microstrip, there is both NEXT and FEXT between two adjacent, coplanar traces. NEXT voltage saturates when the coupled length is greater than one half the risetime of the aggressor, in seconds, times the speed of propagation, in inches per second. For example, at 0.1 nsec risetime and a velocity of 7.7 inches/nsec, the NEXT voltage saturates to a maximum after only 0.385 inches. The only thing to mitigate NEXT is to increase the trace-to-trace spacing and or add a guard trace.

The reduction of FEXT is less dramatic with increased spacing. Slowing the rise time, or decreasing the coupled length, is more effective. Since slowing down the risetime is impractical, the only way to reduce FEXT is to reduce the coupled length, and or add a guard trace.

Since the dielectric surrounding the traces in stripline is more homogeneous, than it is in microstrip, the best way to significantly reduce, or eliminate FEXT, is to route the traces in stripline geometry; if you have that option. Depending on the difference in dielectric constant (*Dk*) between core and prepreg used in the stackup, there is always a probability there will be some small amount of FEXT generated. The best way to mitigate this is to choose cores and prepregs to have similar values of *Dk* when designing the stackup.

By definition, a guard trace is a trace routed coplanar between an aggressor line and a victim line. By doing so, it is believed the guard trace will act as a shield between the aggressor and victim traces. Since it is common practice to specify the line width for the minimum spacing, as a design rule, the separation needs to be three times the line width in order to fit in a guard trace. In this paper, a line width of 5 mils and minimum space of 5 mils is used as a baseline.

Often the guard trace is terminated at each end in its characteristic impedance or shorted to ground. To be most effective though, the guard trace should be shorted to ground, at regular intervals along its length,

using stitching vias, spaced at approximately 1/10th of a wavelength ($\lambda/10$) of the highest frequency component of the aggressor's signal, as illustrated in Figure 5.

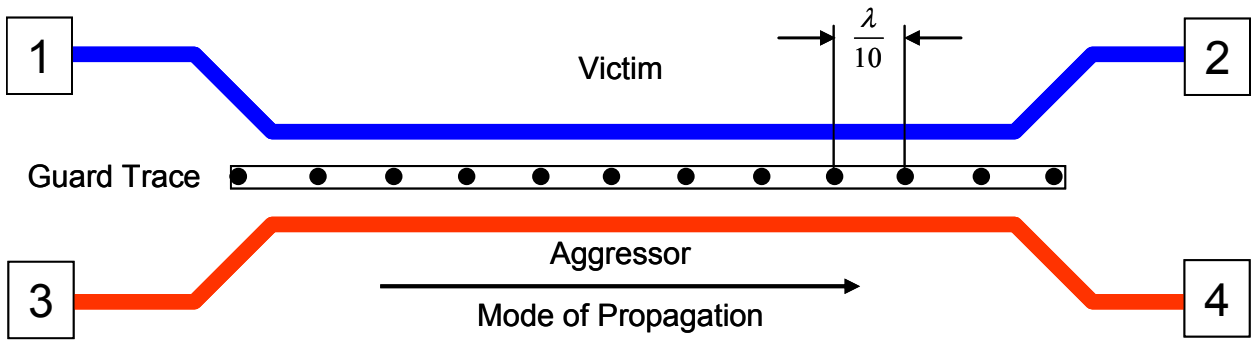

Figure 5 Illustration of guard trace with stitching vias spaced at $\lambda/10$ between aggressor and victim traces.

If the highest frequency component at which the Gaussian impulse response rolls off by 3dB [3] is defined as:

Equation 6

$$f_{3dB} = \frac{0.338}{t_r}$$

Then:

Equation 7

$$\frac{\lambda}{10} = \frac{1}{10 \times f_{3dB}} = \frac{t_r}{3.38}$$

And therefore via stitching spacing is:

Equation 8

$$s_{via} = \frac{t_r}{3.38} \times v = \frac{t_r}{3.38} \times \frac{c}{\sqrt{Dkeff}}$$

Where:

f_{3dB} = Highest frequency component of digital signal –Hz.

t_r = Risetime (10-90%) in sec.

s_{via} = Stitching via spacing in inches.

v = Velocity of signal – inches/sec.

c = Speed of light – 1.18E10 inches/sec.

Dkeff = Effective permittivity or also known as effective dielectric constant surrounding the trace.

Building Simple Scalable Circuit-based Models:

Agilent`s EEsof EDA Design Software (ADS) software [5] was used exclusively to model and simulate the various topologies. The TLines-Multilayer pallet is a 2D field solver with a variety of coupled transmission line models. These models are implemented as the numerical solution of Maxwell's Equations for the two-dimensional cross-section geometry that is defined by the model parameters.

Modeling Methodology:

The methodology used for this study was to build four parameterized coupled transmission line topologies:

Topology 1 - Microstrip without a guard trace
Topology 2 - Microstrip with a guard trace
Topology 3 - Stripline without a guard trace
Topology 4 - Stripline with a guard trace

In order to be able to simulate a guard trace with stitching vias, topologies 2 and 4 were built with 6 sections of ML3CTL_V (3 Coupled Lines, Variable Width and Spacing) transmission line models as shown in Figure 6. The length of each section was parameterized to facilitate changing the stitching via spacing. The stitching vias and the end-termination resistors can be deactivated and/or shorted as required. A 0-1V VtStep source, with a parameterized risetime, was used for transient analysis.

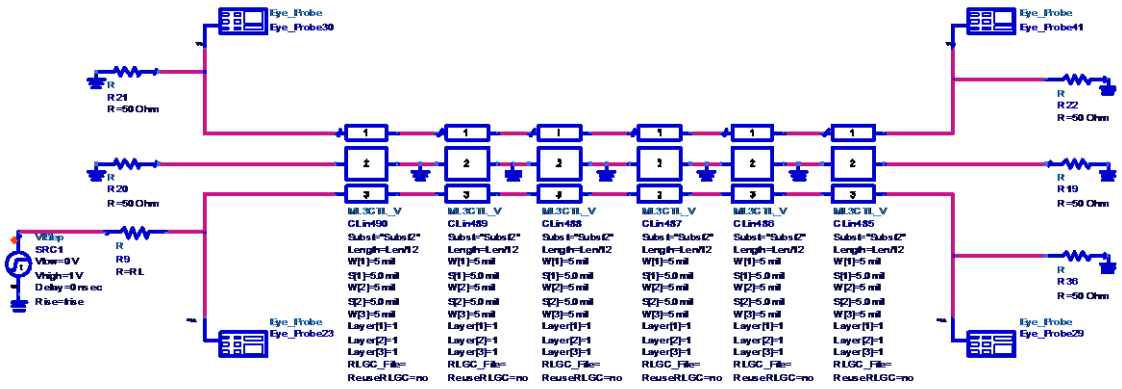

Figure 6 Example of generic circuit model for topologies with guard traces.

Topologies 1 and 3 were built with 6 sections of ML2CTL_V (2 Coupled Lines, Variable Width and Spacing) transmission line models as shown in Figure 7. Both the length and spacing between tracks were parameterized in order to easily adjust to agree with topologies 2 and 4 for comparisons. Similarly, the same VtStep source was used for transient analysis.

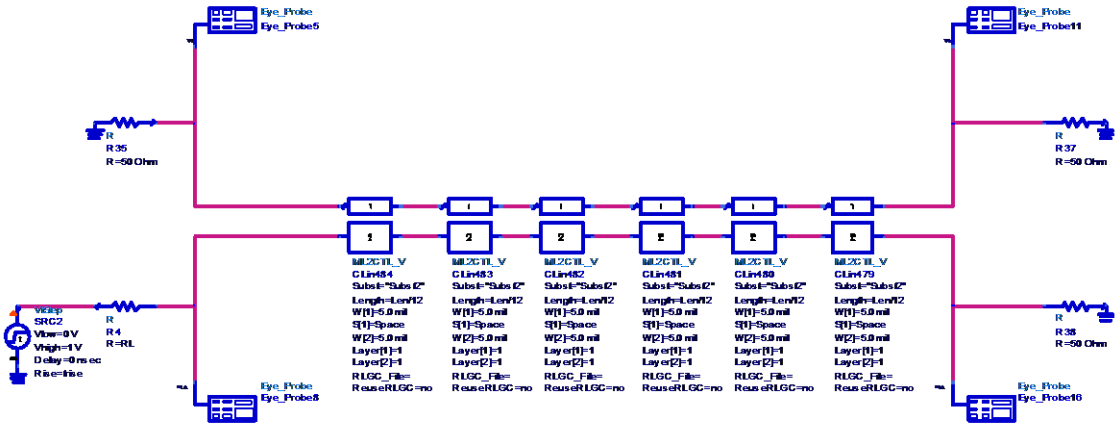

Figure 7 Example of generic circuit model for topologies without guard traces.

To complete the circuit models, two multi-layer substrates were used to define the stack-up parameters as shown in Figure 8.

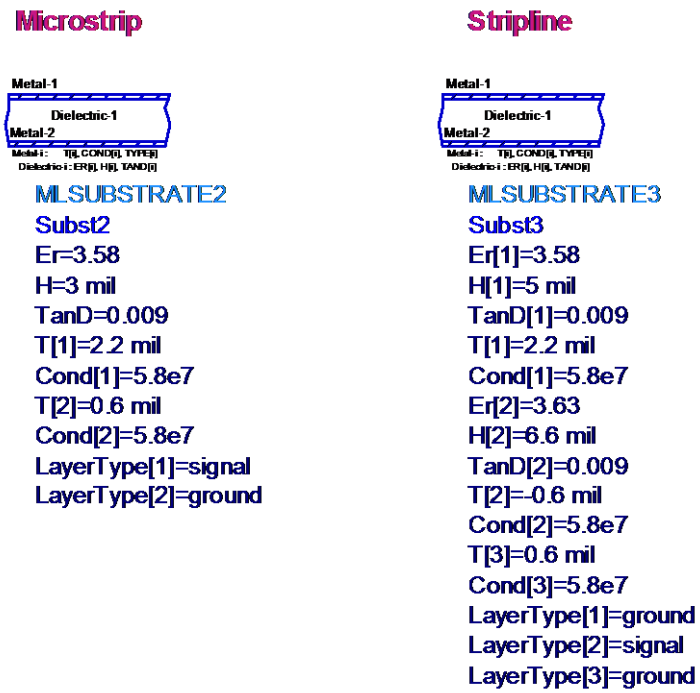

Figure 8 Multi-layer substrates used in this study. Subst2 show stack-up parameters for microstrip, and Subst3 is for stripline.

Case Study Parameters:

Dkeff Stripline = 3.61 (Average value 3.58; 3.63 -Figure 8)

Dkeff Microstrip = 2.29 (Average value 3.58; Air(1) -Figure 8)

Risetime = 100 psec

Minimum Line width /space = 5 mils

Length = 1.5 inches

Dissipation factor = *Df* = 0.009

With an effective dielectric constant of 2.29 for microstrip and 3.61 for stripline, the stitching via spacing worked out to be 231 mils and 184 mils using Equation 8 respectively. Comparing 6 sections at 250 mils vs 8 sections at 187 mils in stripline, the difference in NEXT is less than 0.01%. For the sake of simplicity, a via stitching spacing of 250 mils was used for all microstrip and stripline topologies.

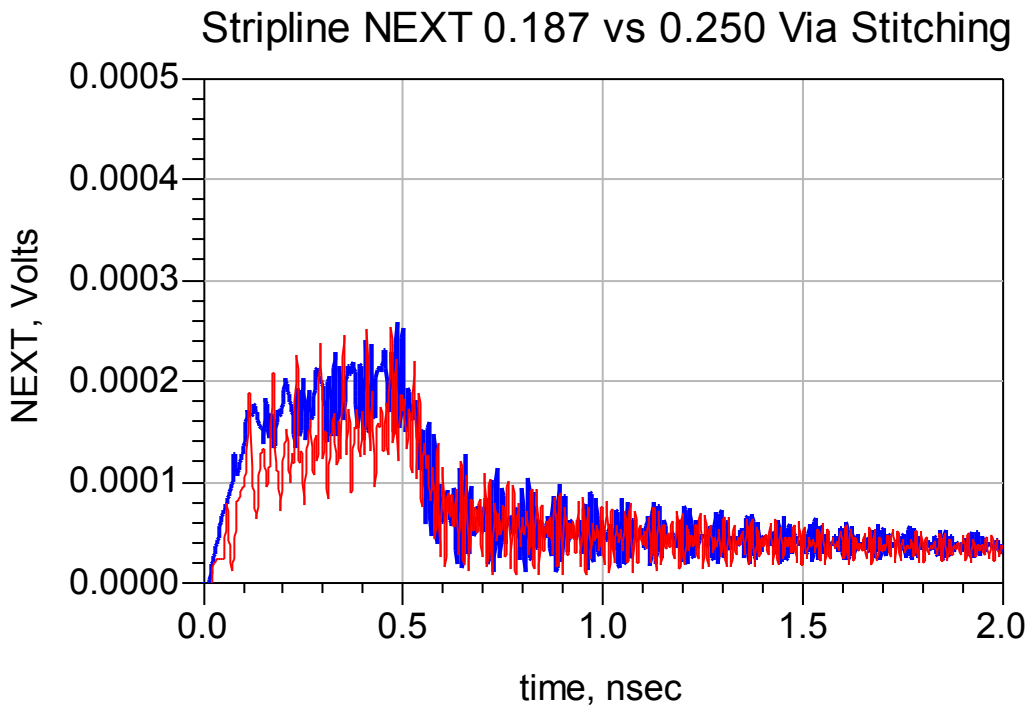

Figure 9 Stripline NEXT comparison. Via stitching 250 mils (blue) vs 187 mils (red). With aggressor voltage of 0.5V, NEXT delta is less than 0.01%.

Simulation Cases:

With the caveat that in order to fit a guard trace between an aggressor and victim, the separation needs to be at least three times the line width, a spacing of 15 mils was used between the aggressor and victim tracks for all cases. For topologies 2 and 4, a 5 mil track was used centered between the two tracks.

The following is a list of transient simulation cases for microstrip and stripline topologies; comparing NEXT and FEXT; guarded vs non-guarded trace:

Case 1: No guard trace. - 5 mil space baseline.
Case2: Guard Trace terminated in 50 Ohms each end.
Case3: Guard Trace GND each end.
Case4: Guard Trace stitched at 250 mils

Data and Results:

Case 1 No guard trace. - 5 mil Space Baseline:

When the topology shown in Figure 7 was configured for stripline and microstrip scenarios, the results for Case 1 are summarized in Figure 10. The spacing was set to 5 mil separation, and risetime set to 100 psec. NEXT is 6.7% for microstrip vs 5.3% for stripline, while FEXT is 10.6% for microstrip vs 0% for stripline. As expected, the NEXT and FEXT is worse for microstrip.

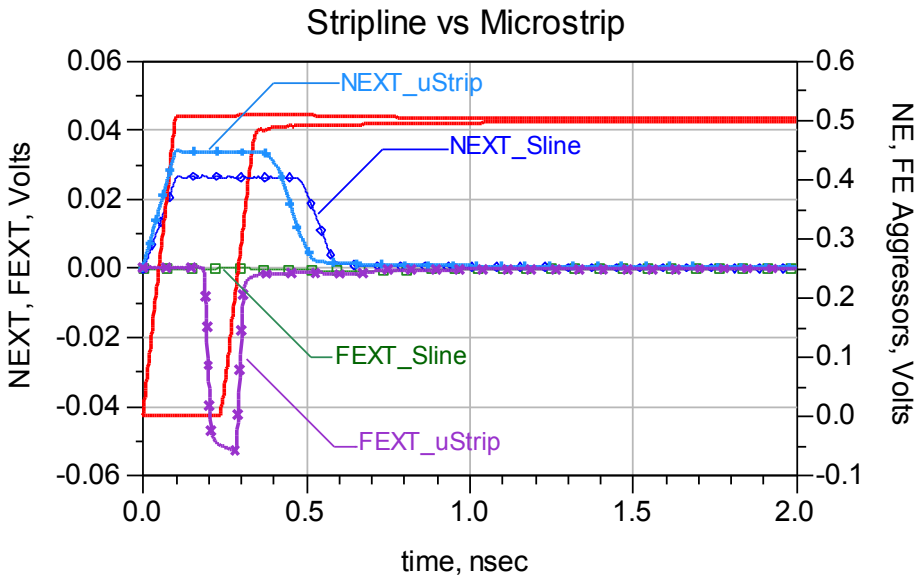

Figure 10 Simulation results, in response to a step edge aggressor, for Case 1. Stripline vs Microstrip NEXT, FEXT comparison. No guard trace, 5 mil space. Simulated and plotted with Agilent ADS.

Case 2 Guard Trace terminated in 50 Ohms Each End:

The topologies shown in Figure 6 and Figure 7 were configured for stripline and microstrip. The 50 Ohm terminations were left activated, and stitching vias were deactivated as required. The spacing was set to 15 mils for topologies 1 & 3 without guard trace, and 5 mils for topologies 2 & 4 with guard trace. Risetime set to 100 psec.

The results are presented in Figure 11. The top left plot compares microstrip NEXT; with and without a guard trace. The near-end aggressors are included for reference. Although NEXT is slightly better with the guard trace, up to 0.35 nsec, the additional pulse at 0.45 nsec negates the benefit overall. This pulse is actually FEXT from the falling edge of NEXT on the guard trace as shown in Figure 12 left.

The top right plot, of Figure 11, compares microstrip FEXT with and without a guard trace. The far-end aggressors are included for reference. As was the case with NEXT, the FEXT is slightly better except for the positive and negative spikes. These spikes are also caused by FEXT on the far-end guard trace as shown in Figure 12 right.

The bottom left plot, of Figure 11, compares stripline NEXT with and without a guard trace. The near-end aggressors are included for reference. The results show NEXT with a guard trace is slightly better (0.3%) than NEXT without a guard trace (0.33%). The reason is the incident step waveform, Va, couples NEXT onto the guard trace, which in turn couples NEXT onto the victim. For example, using the results from Case 1, 5.3% of Va (0.53V) is coupled onto the guard trace, which in turn couples 5.3% of the result onto the victim as shown below:

$(Kb \times Va) \times Kb = (0.053 \times 0.53) \times 0.053 = 1.49\ mV$; compared to the measured voltage of 1.51mV.

The bottom right plot, of Figure 11, compares stripline FEXT with and without a guard trace. The far-end aggressors are included for reference. As expected, in stripline, there is no FEXT pulse coincident with the far-end aggressor's rising edge. The FEXT waveform with a guard trace, that is shown, is a result of the high to low transition of the NEXT pulse on the guard trace at the far-end; effectively coupling a negative going NEXT pulse for a duration of 2TD. The clue is that this waveform has essentially the same magnitude (only negative) as the NEXT waveform, shown in bottom left.

The FEXT, with no guard trace waveform, is actually a reflection due to slight impedance mismatch at the far-end. As an experiment, when the termination resistor was increased to 60 Ohms, the FEXT with no guard trace had a positive going reflection; while the FEXT, with guard trace, did not change.

In summary, adding a guard trace, terminated at both ends with 50 Ohms, does little to improve crosstalk on the victim. In fact, for three of the four scenarios, it was slightly worse.

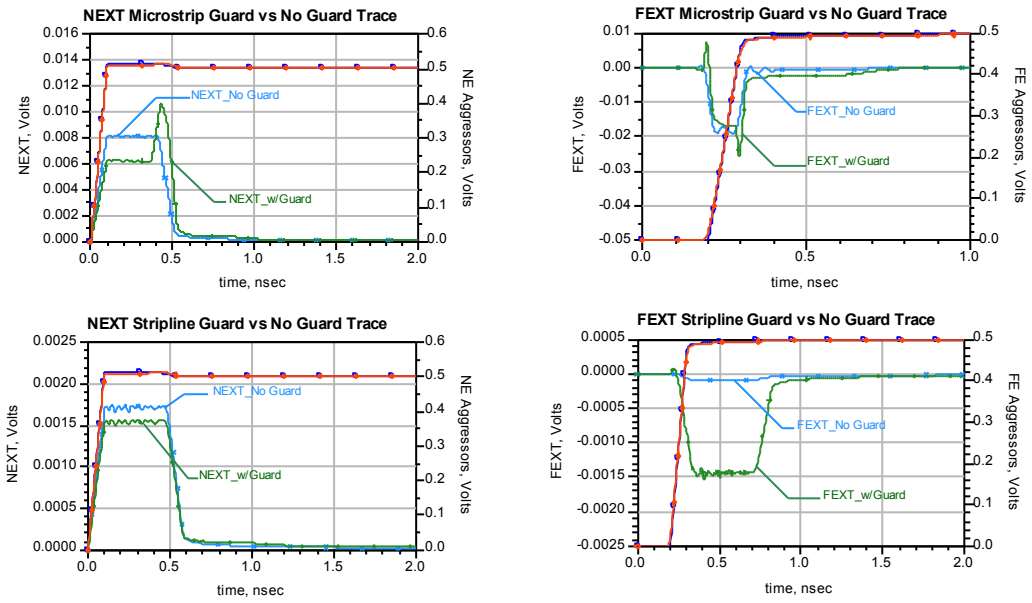

Figure 11 Simulation results for Case 2. Microstrip vs Stripline; NEXT, FEXT comparisons; with and without guard traces; 50 Ohm terminated. Adding a guard trace terminated in 50 Ohms, does little to improve crosstalk on the victim. In fact in three of the four scenarios, it is slightly worse. Simulated and plotted with Agilent ADS.

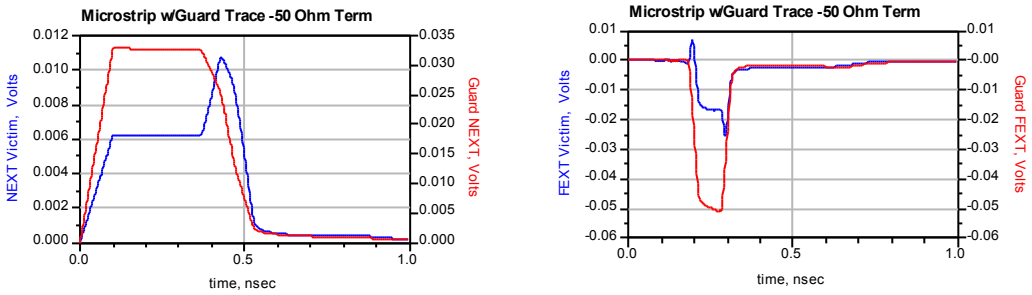

Figure 12 Simulation results for Case 2. On the left, the red trace is NEXT on the guard trace and the blue is NEXT of the victim. The positive spike is FEXT due the falling edge of the NEXT on the guard trace. Similarly, on the right, the positive and negative spikes, on the FEXT victim (blue), are caused by FEXT from the FEXT pulse (red) on the guard trace at the far-end. Simulated and plotted with Agilent ADS.

Case 3 Guard Trace GND Each End:

The topologies shown in Figure 6 and Figure 7 were configured for stripline and microstrip. The 50 Ohm terminations were shorted and stitching vias were deactivated as required. The spacing was set to 15 mils for topologies 1 & 3 without guard trace, and 5 mils for topologies 2 & 4 with guard trace. Risetime set to 100 psec.

The results are presented in Figure 13. The top two plots compares microstrip NEXT and FEXT; with and without a guard trace respectively. The near-end and far-end aggressors are included for reference. The damped oscillating crosstalk, in both plots, are a result of the two spikes originating on the FEXT pulse; as shown in the top right plot. Because the ends are grounded, the FEXT pulse and voltage spikes are reflected at each end. The amplitude decays to a small ripple after about ten round-trip delays as shown in Figure 14.

The bottom left plot, of Figure 13, compares stripline NEXT with and without a guard trace. The near-end aggressors are included for reference. In this case, NEXT with a guard trace is significantly better (0.05%) than NEXT without a guard trace (0.33%).

The bottom right plot, of Figure 13, compares stripline FEXT with and without a guard trace. The far-end aggressors are included for reference. As expected, in stripline, there is no FEXT pulse coincident with the far-end aggressor's rising edge. The guard trace provides no improvement at the far-end.

In summary, adding a guard trace grounded at each end, does little to improve crosstalk on the victim in all cases except NEXT in stripline. In fact, in microstrip, it was actually worse.

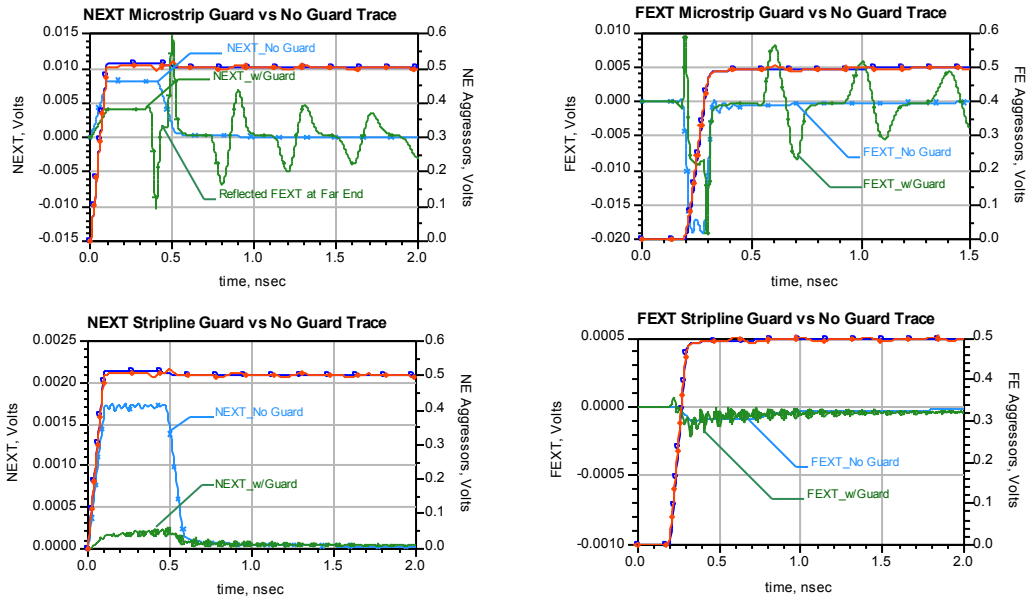

Figure 13 Simulation results for Case 3. Microstrip vs Stripline; NEXT, FEXT comparisons; with and without guard traces grounded at each end. Adding a guard trace, does little to improve crosstalk on the victim in all cases except NEXT in stripline, In fact in microstrip, shows it is actually worse in both cases. Simulated and plotted with Agilent ADS.

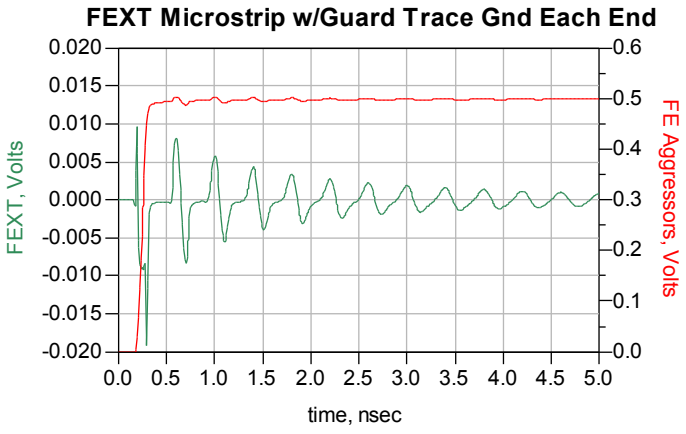

Figure 14 Simulation results for Case 3 microstrip FEXT on victim with guard trace grounded at both ends. Because the ends are grounded, the FEXT pulse and voltage spikes are reflected at each end. The amplitude decays to a small ripple after about ten round-trip delays. Simulated and plotted with Agilent ADS.

Case 4 Guard Trace GND Stitched:

The topologies shown in Figure 6 and Figure 7 were configured for stripline and microstrip. The 50 Ohm terminations and stitching vias were activated as required. The spacing was set to 15 mils for topologies 1 & 3 without guard trace, and 5 mils for topologies 2 & 4 with guard trace. Risetime set to 100 psec.

The results presented in Figure 15 are similar to Case 3, except the oscillations shown on the NEXT and FEXT microstrip plots are less in amplitude, and FEXT decays to a small ripple within two round-trip delays after the far-end aggressor.

Even though there is ringing superimposed on the NEXT waveform with guard trace, in microstrip, it is still slightly better than NEXT without a guard trace. At the far end, FEXT is reduced by approximately 50% by adding a guard trace.

For Stripline, the ground stitching offers is no improvement in NEXT or FEXT compared to Case 3. In fact, the results are essentially the same.

In summary, adding a guard trace with ground stitching, improves crosstalk in all four scenarios.

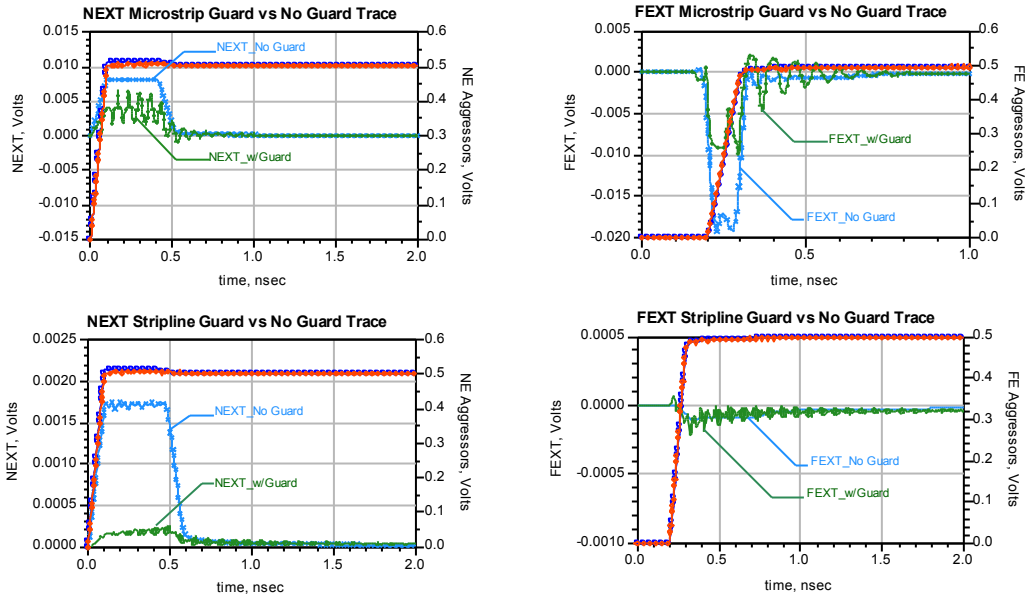

Figure 15 Simulation results for Case 4. Microstrip vs Stripline; NEXT, FEXT comparisons; with and without guard traces stitched to ground. Adding a guard trace with ground stitching, improves crosstalk in three of the four scenarios. Since there is no FEXT in stripline, there is no room for improvement. Simulated and plotted with Agilent ADS.

Eye Analysis:

In order to quantify just how much a guard trace improves crosstalk, in digital applications, a channel eye analysis was done on Case 4 (GND stitching) using Agilent ADS's Channel Simulator feature. Four topologies were constructed; as shown in the sample channel topologies of Figure 16. Only two topologies (microstrip) are shown because the other two (stripline) are exactly the same except for the coupled line segments refer to a different MLSUBSTRATE as was shown in Figure 8.

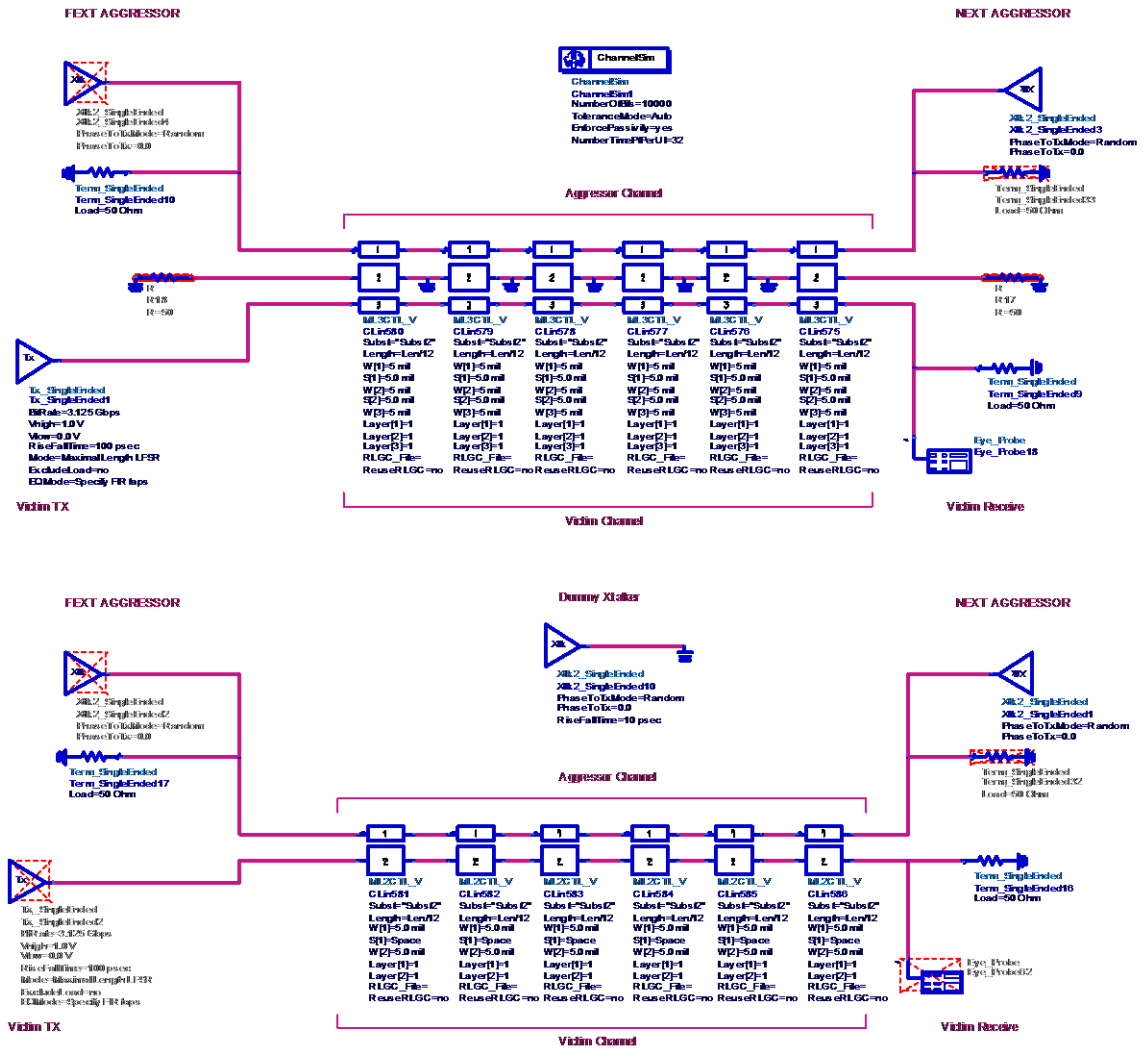

Figure 16 Sample topologies modeled in Agilent ADS used for eye analysis using ChannelSim feature. Top topology is for microstrip with guard trace stitched to ground at 0.25 inches compared to microstrip without a guard trace spaced at 15 mils. Both are configured for NEXT simulation, with the top one being active. The termination resistors at the end of each end of the guard trace are deactivated and shorted to ground. The dummy crosstalker ensures the max time step is forced to risetime/2; where risetime is the shortest risetime of the Tx/Xtalker's that are active. Modeled with Agilent ADS.

The topologies were built with all aggressors and terminators connected. The bit-rate was set to 3.125 GB/s with a rise and fall time equal to 100 psec. The voltages of all drivers were set to 0-1V. Because ChannelSim feature of ADS only allows one transmitter to be active, only one topology could be analyzed at a time. Therefore, the respective transmitters were deactivated during simulation. The crosstalk drivers and associated terminations were also deactivated as required for the respective simulation. For the example shown, the topologies are set up for NEXT evaluation, with the top topology (ground-stitched guard trace) being active.

The dummy Xtalker, shorted to ground, ensures the max time step is forced to risetime/2; where risetime is the shortest risetime of the Tx/Xtalker's that are active. Its risetime was set to 10 psec.

Data and Results:

A summary of the eye analysis for Case 4 is presented in Table 1 and Figure 17. The actual eye diagrams are shown in the appendix. As expected, microstrip shows more improvement over stripline when the trace-trace separation was 15 mils. In terms of eye height, adding a ground-stitched guard trace reduces NEXT and FEXT by 6 mV and 22 mV respectively, while only improves stripline NEXT by 3 mV.

When the space was increased to 25 mils, to the topology with no guard trace, the results for microstrip showed NEXT was better by 3mV, and FEXT was worse by only 2mV. In stripline, it was no further improvement in NEXT or FEXT

In terms of eye width, adding a ground-stitched guard trace to microstrip shows no improvement for NEXT and only 3.2 psec for FEXT. For stripline there was 3.2 psec improvement for NEXT and FEXT.

When the space was increased to 25 mils, to the topology with no guard trace, the results for microstrip showed NEXT was better by 3.2 psec, but no better for FEXT when compare to the case with a guard trace. In stripline, it was no improvement in NEXT or FEXT.

In summary, when the trace-trace spacing was 3 times the line width, adding a ground-stitched guard trace reduced crosstalk and improved jitter slightly. However, by increasing the spacing to 5 times line width, and leaving the guard trace spacing equal to the line width, the crosstalk and jitter, for all intensive purposes, was the same.

Table 1 Eye Simulation Comparing Results for Case 4 Ground-stitched Guard Trace vs No Guard Trace.

Simulation	Eye Height mv	Delta mv	Eye Width psec	Delta psec
uStrip NEXT w/Guard	479		315.2	
uStrip NEXT no Guard 15 mil space	473	-6.0	315.2	0.0
uStrip NEXT no Guard 25 mil space	482	3.0	318.4	3.2
uStrip FEXT w/Guard	475		315.2	
uStrip FEXT no Guard 15 mil space	453	-22.0	312.0	-3.2
uStrip FEXT no Guard 25 mil space	473	-2.0	315.2	0.0
Stripline NEXT w/Guard	488		320.0	
Stripline NEXT no Guard 15 mil space	485	-3.0	316.8	-3.2
Stripline NEXT no Guard 25 mil space	488	0.0	320.0	0.0
Stripline FEXT w/Guard	488		318.4	
Stripline FEXT no Guard 15 mil space	488	0.0	318.4	0.0
Stripline FEXT no Guard 25 mil space	488	0.0	318.4	0.0

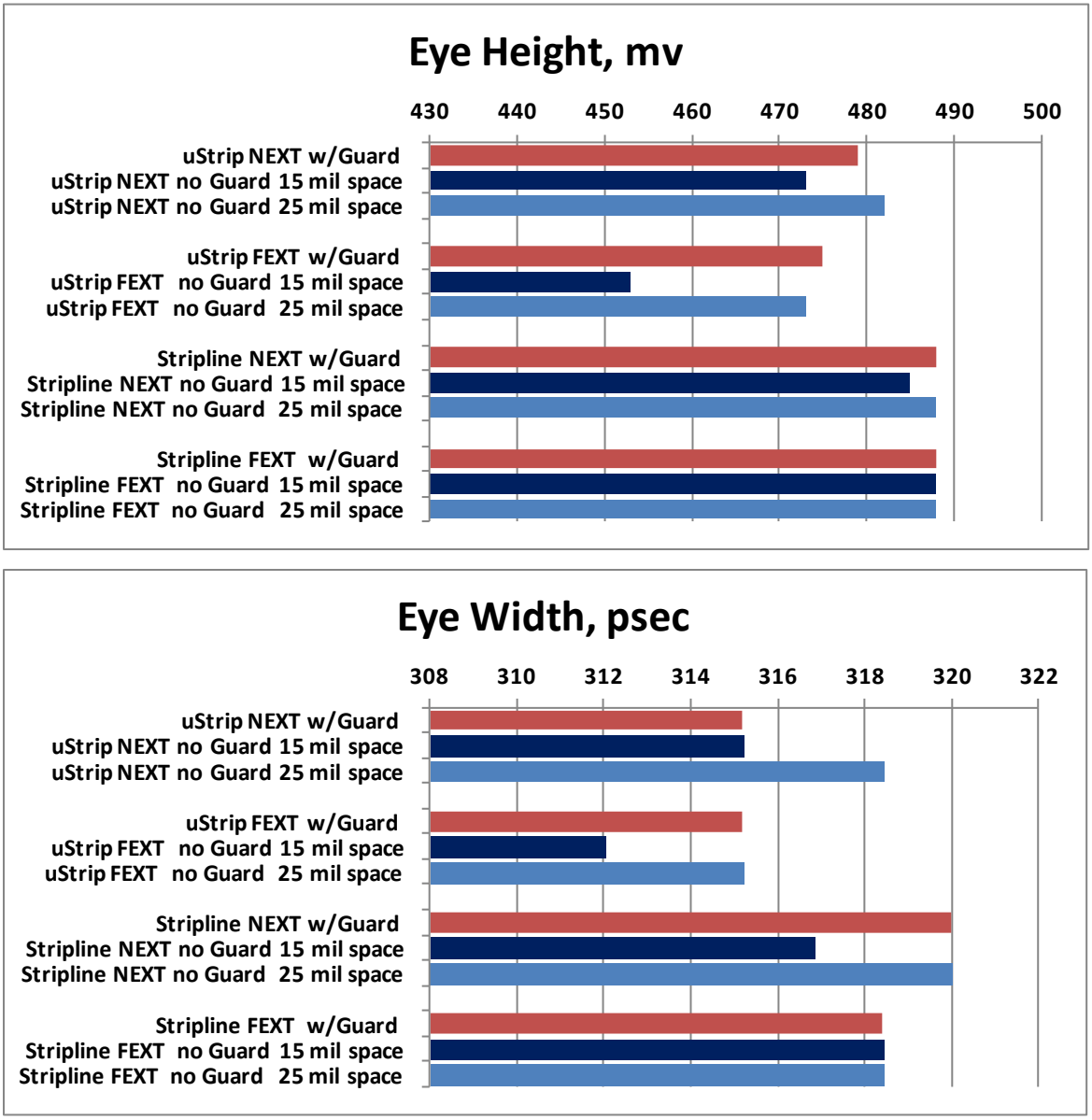

Figure 17 Eye Simulation Comparing Results for Case 4 Ground-stitched Guard Trace vs No Guard Trace. In all cases, the scenarios with a guard trace, the spacing between the three traces was 5 mils compared to 15 mils and 25 mils without guard trace.

Follow-up Microstrip Study:

After publishing the original paper, there was a comment and request to see the effect of increasing the dielectric thickness for the microstrip scenario. The argument is that since the dielectric thickness originally used was only 3 mils and the track to guard spacing was 5 mils, most of the signal return current goes through the ground plane rather than through the guard trace. By increasing the dielectric thickness, to say 15 mils, and using a properly stitched guard trace, there would be more of an improvement observed.

It should be pointed out that in this study, the goal was trying to keep 50 Ohm impedance the same between stripline and microstrip for the same line width and spacing. This was done in order to compare apples to apples, and to get close to a real-world practical example stackup. If we are concerned about microstrip only, and not worrying about maintaining 50 Ohm impedance, then, by varying the height, it will of course show different results.

The key will be what knobs need to change to keep the same impedance? To maintain 50 ohms, when the dielectric is increased, the track width needs to be wider. By maintaining the same geometry and merely increase the dielectric, the impedance will be higher; which will result in an overshoot to the original aggressor step waveform for 2TD for 50 ohm termination. This overshoot also tends to increase the NEXT and FEXT.

With that in mind, an experiment was set up to increase the dielectric height to 15 mils, then simulate the following scenarios, and compare against the baseline:

1. Scenario 1: Baseline; 3 mil dielectric; 5 mil tracks; 5 mil stitched guard trace; 5 mil space.
2. Scenario 2: 15 mil dielectric; 5 mil tracks; 5 mil stitched guard trace; 5 mil space.
3. Scenario 3: 15 mil dielectric; 25 mil tracks; 5 mil stitched guard trace; 5 mil space.
4. Scenario 4: 15 mil dielectric; 25 mil tracks; 20 mil stitched guard trace; 5 mil space.
5. Scenario 5: 15 mil dielectric; 25 mil tracks; 65 mil stitched guard trace; 5 mil space.

Scenario 1 is the baseline originally used for comparison to the other scenarios. Scenario 2 is exactly the same as scenario 1, except that the height is increased to 15 mils. Scenario 3 keeps a 5 mil guard trace, but increases the track width to 25 mils to get to approximately 50 Ohm impedance.

Scenario 4 increases the guard trace to minimum 20 mils; equal to the pad diameter of the stitching vias. It is a more practical scenario because the 15 mil dielectric would cause the drill size to increase to 8 mils in order to deal with the higher aspect ratio. At 3 mil dielectric height, it was assumed a 4 mil laser drilled micro-via could be used for stitching the 5 mil guard trace.

Scenario 5 increases the overall space between the victim and aggressor to 3 times the line width (75 mils total). This allows for a 65 mil guard trace with 5 mil gap on each side. This is the best for comparison to the baseline and to confirm the 3 times line width separation rule of thumb.

Data and Results:

The results of the simulations are shown in Figure 18 to Figure 22. The left-side plots, in each figure, are NEXT. The right-side plots are FEXT. The scales were kept the same to better compare at a glance.

By just increasing the dielectric thickness to 15 mils, as shown in Figure 19, the near-end and far-end crosstalk, without guard trace, is considerably worse, as expected, particularly due to the impedance mismatch.

Figure 20 shows that when the track width was increased to 25 mils, to better match the transmission line impedance, the spikes and step in the crosstalk signatures have been eliminated. But the crosstalk, for non-guarded case, is still about double.

When the spacing was increased to 30 mils and guard trace increased to 20 mils, as shown in Figure 21, the crosstalk reduces proportionately.

But when the spacing increases to 3 times the line width spacing, as shown in Figure 22, the crosstalk is comparable to the baseline results of Figure 18; even though the dielectric thickness has increased. This seems to suggest that as long as the geometry is scaled to the same proportion to achieve 50 Ohms, and the spacing between victim and aggressor is also scaled by the same proportion, to 3 times the line width, the crosstalk will have the same order of magnitude.

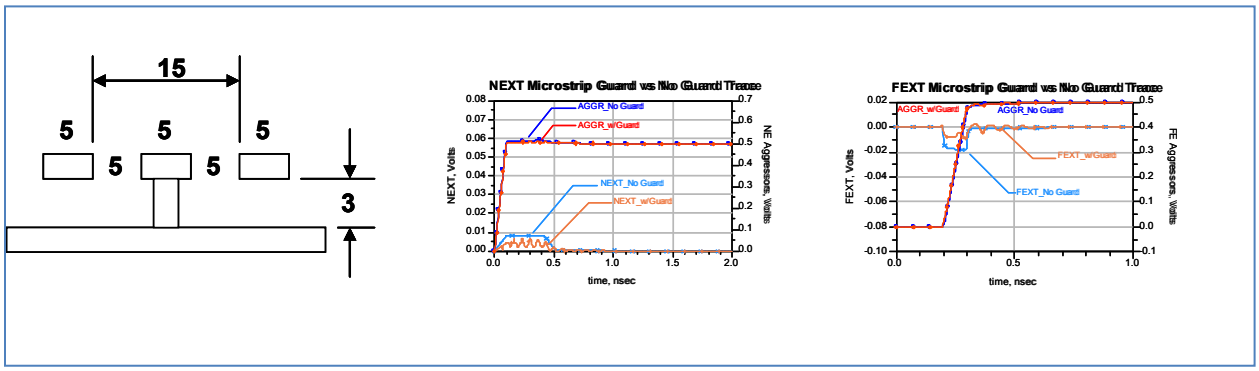

Figure 18 Scenario 1. Baseline microstrip geometry. The left plot is NEXT and the right plot is FEXT. The respective aggressors are shown for reference. Simulated with Agilent ADS.

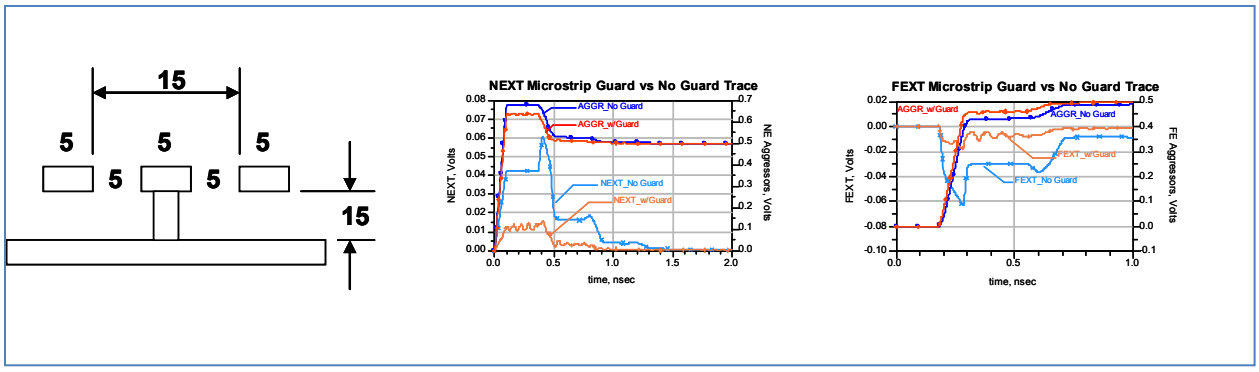

Figure 19 Scenario 2 Dielectric height increased to 15 mils, keeping all other parameters the same. The spikes and step in the NEXT and FEXT signatures are due to the impedance mismatch as seen by the Aggressor waveforms. Simulated with Agilent ADS.

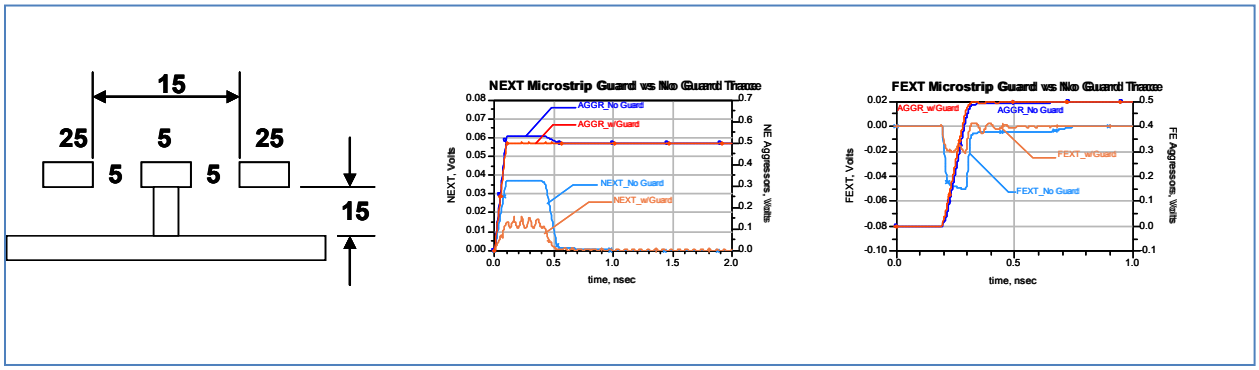

Figure 20 Scenario 3. Line width increased to 25 mils to better match impedance to 50 Ohms. Absence of spikes and step in the crosstalk signatures confirm they were originally due to impedance mismatch as observed in scenario 2. Simulated with Agilent ADS.

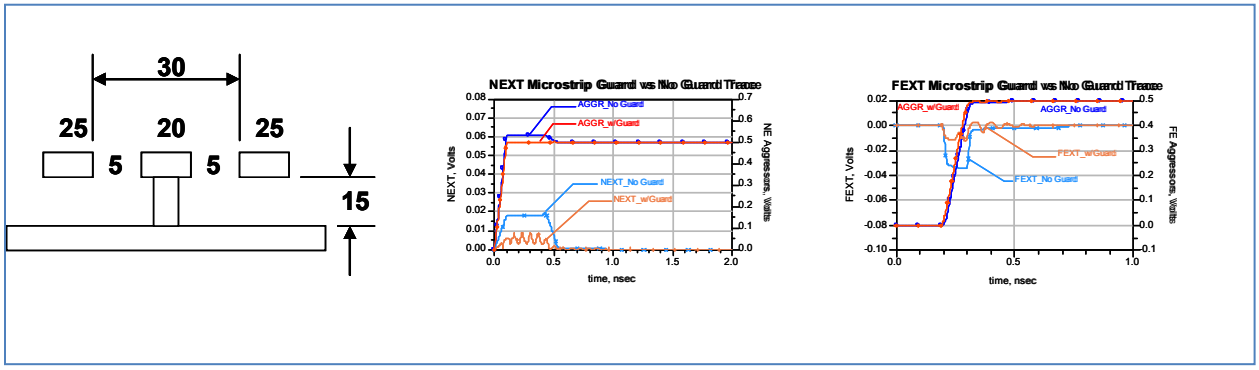

Figure 21 Scenario 4 Spacing increased to 30 mils to allow a 20 mil guard trace with 5 mil gap each side. Crosstalk is reduced in both cases proportionally. Simulated with Agilent ADS.

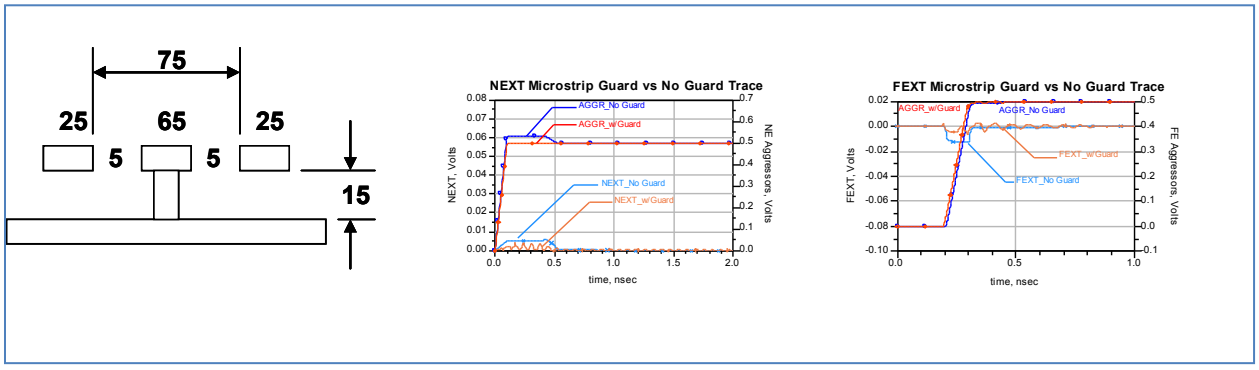

Figure 22 Scenario 5 Space increased to 3 times line width and guard trace increased to 65 mils to maintain 5 mil gap each side. NEXT and FEXT is comparable to the baseline case in Figure 18. Simulated with Agilent ADS.

Summary and Conclusion:

Adding a guard trace, terminated at both ends with 50 Ohms, does little to improve crosstalk on the victim. In fact in three of the four scenarios, it was slightly worse. The same was true when the guard trace was grounded at each end.

Adding a guard trace with ground stitching improves NEXT in both microstrip and stripline topologies, and only improves FEXT in microstrip. Since there is no FEXT in stripline, there is no improvement.

The follow-up microstrip study has proven that changing the height of the dielectric has no effect on the magnitude of crosstalk when the spacing is also scaled to 3 times the line width; as long as the rest of the geometry is scaled to the same proportion to achieve 50 Ohms.

When eye diagrams were compared, the results were consistent with the transient step response analysis. Microstrip eye analysis shows more improvement in crosstalk over stripline when the trace-trace separation was 3 times the line width, however, when space was increased to 5 times the line width, the results were essentially the same.

In conclusion, this study has shown that when trace-trace spacing in microstrip is 3 times the line width, adding a ground-stitched guard trace reduces crosstalk and improves jitter slightly. It is the best solution if a guard trace were to be used. However, by increasing the spacing to 5 times line width, and leaving the guard trace spacing equal to the line width, the crosstalk, for all intensive purposes, is the same. In stripline, there is essentially no benefit in adding a guard trace for digital signaling.

To guard or not to guard? That was the original question. The answer of course is, "*It Depends*". Certainly in microstrip there showed some improvement when the guard trace was stitched to ground at ($\lambda/10$), but in stripline there was really no benefit for the same spacing. This case study has shown that by increasing the spacing to five times the line width, in microstrip, and three times the line width, in stripline, it is a good, practical rule of thumb to use; instead of adding a stitched guard trace. Personally, what I do is to use a 2D field solver to adjust the spacing until the odd-mode impedance approximately equals the even-mode impedance. The answer is always less than 1%.

Appendix:

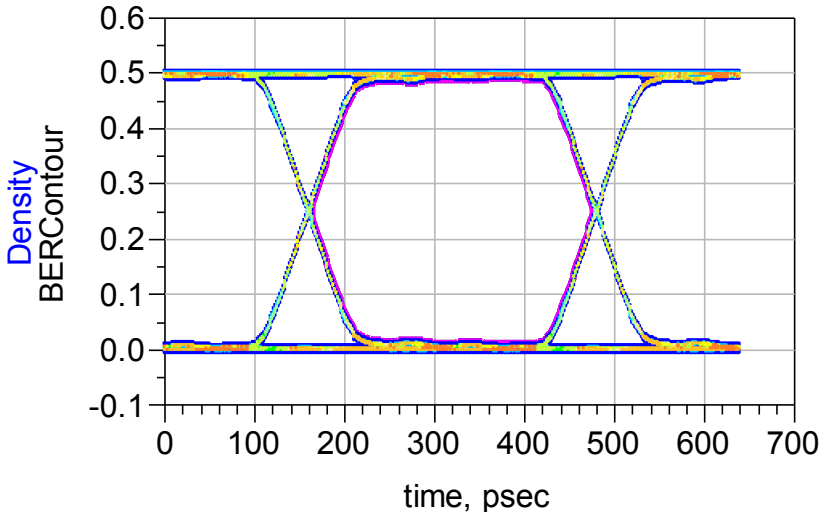

Figure 23 uStrip NEXT w/guard

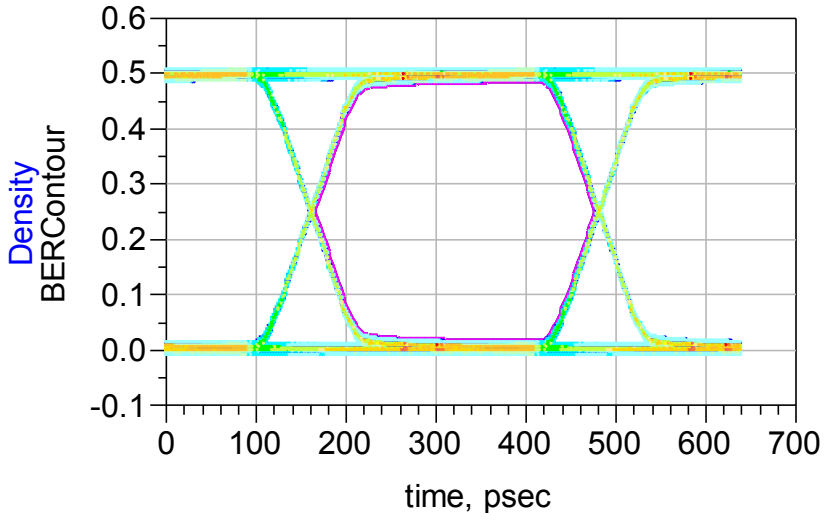

Figure 24 uStrip NEXT no Guard15 mil spacing.

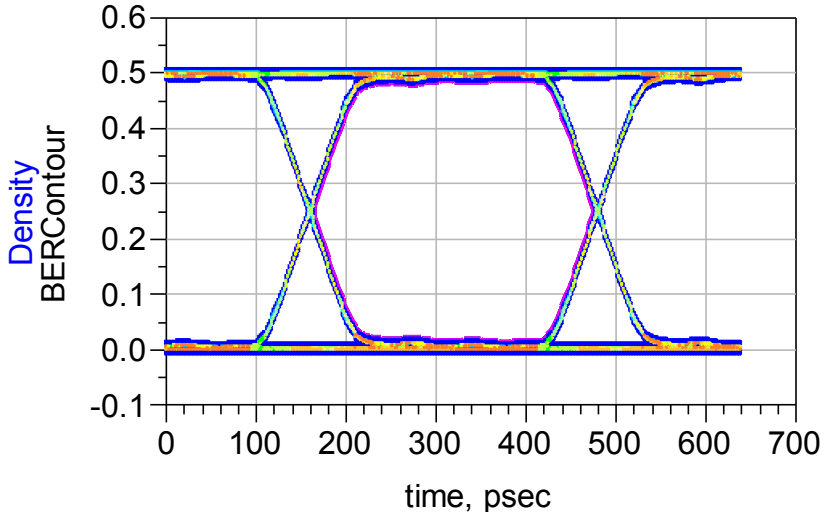

Figure 25 uStrip FEXT w/guard

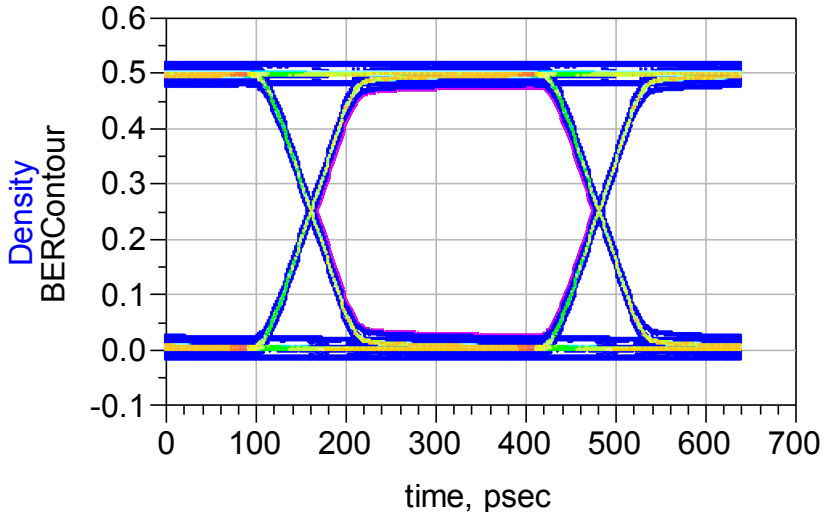

Figure 26 uStrip FEXT no guard15 mil spacing.

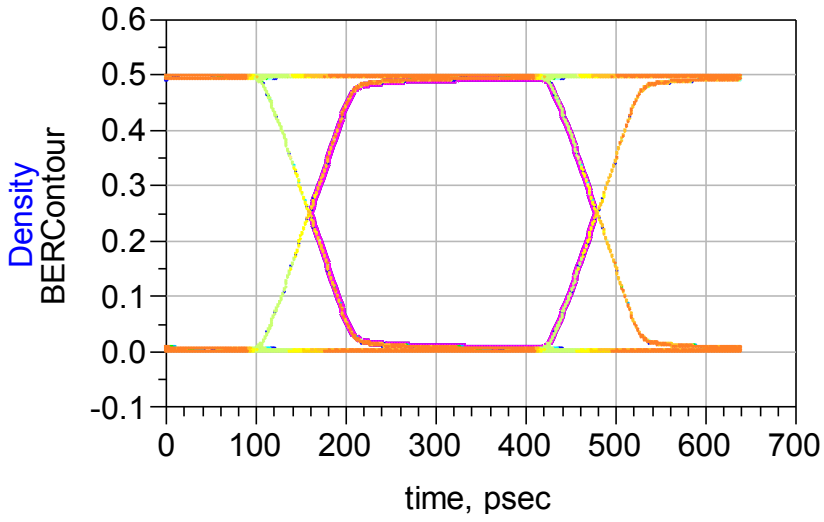

Figure 27 Stripline NEXT w/guard

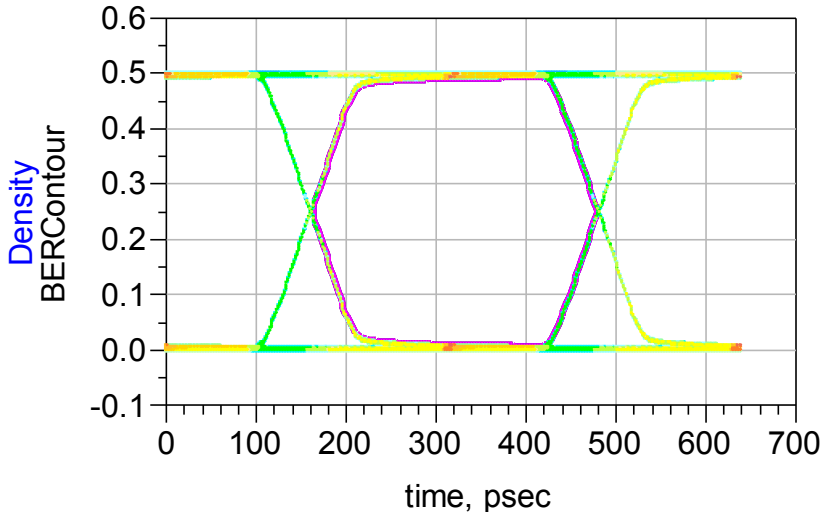

Figure 28 Stripline NEXT no Guard 15 mil spacing.

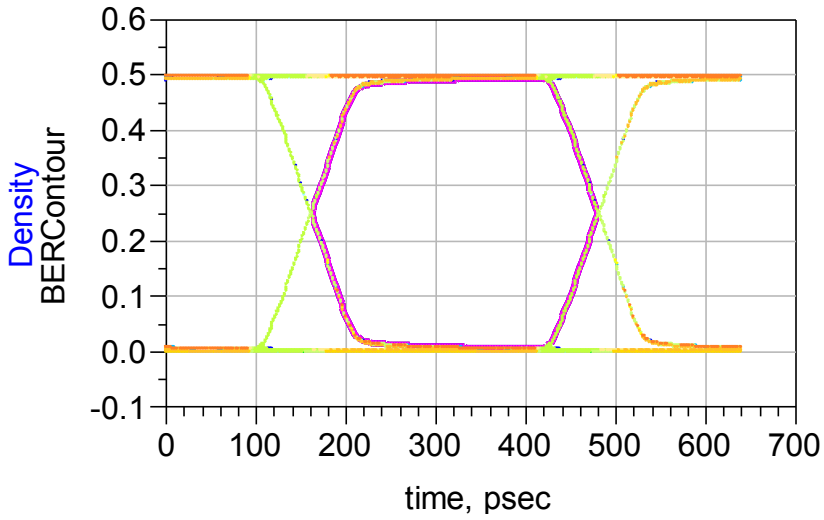

Figure 29 Stripline FEXT w/guard

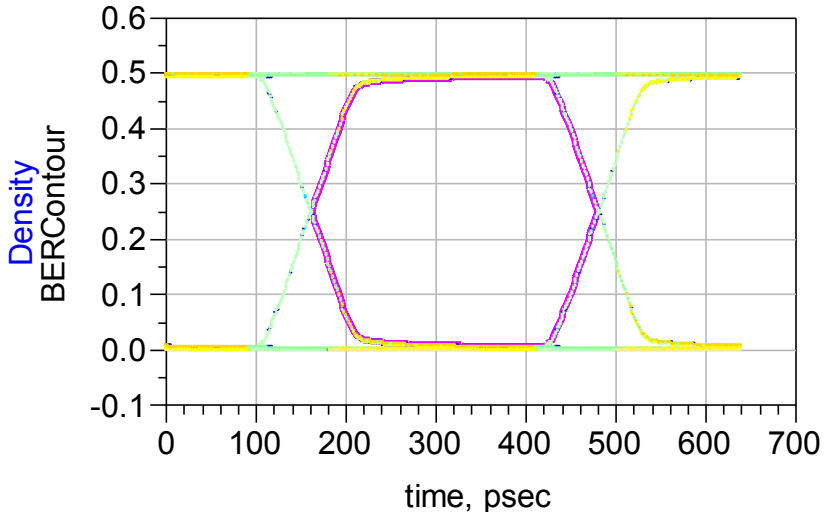

Figure 30 Stripline FEXT no guard 15 mil spacing.

Eye diagrams with Spacing 25 mils:

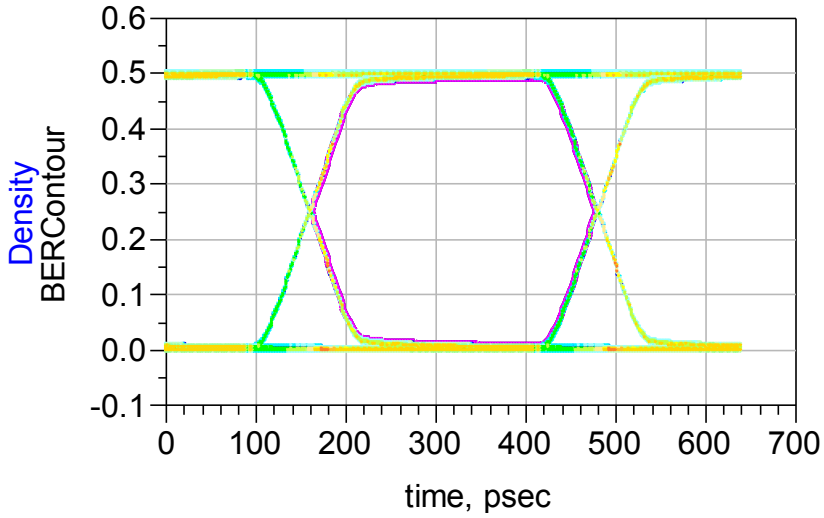

Figure 31 uStrip NEXT no Guard 25 mil space.

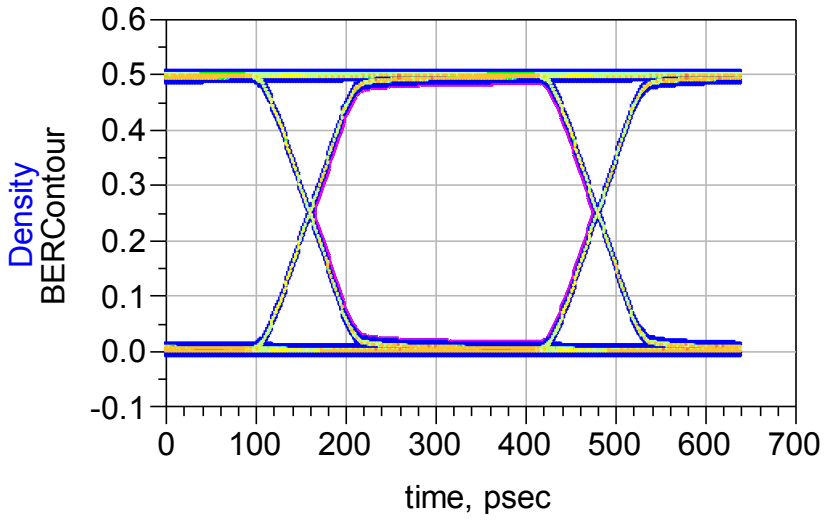

Figure 32 uStrip FEXT no guard 25mil space.

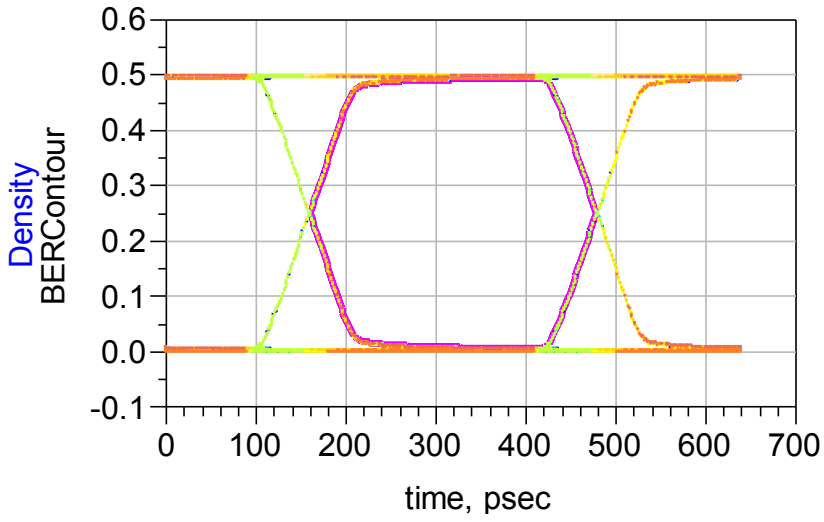

Figure 33 Stripline NEXT no Guard 25 mil space.

References:

[1] E. BOGATIN, " SIGNAL INTEGRITY SIMPLIFIED", PRENTICE HALL PTR, 2004
[2] H. JOHNSON, M. GRAHAM, "HIGH-SPEED SIGNAL PROPAGATION", PRENTICE HALL PTR, 2003
[3] H. JOHNSON, M. GRAHAM, "HIGH-SPEED DIGITAL DESIGN", PRENTICE HALL PTR, 1993
[4] W.R.BLOOD, JR., "MECL SYSTEM DESIGN HANDBOOK",MOTOROLA INC., 1983
[5] Agilent Technologies, EEsofEDA, Advanced Design System, 2009 Update1 software.

Bibliography

Lambert (Bert) Simonovich graduated in 1976 from Mohawk College of Applied Arts and Technology in Hamilton, Ontario, Canada as an Electronic Engineering Technologist. Over a 32 year career at Bell Northern Research and Nortel, he helped pioneer several advanced technology solutions into products and has held a variety of R&D positions; eventually specializing in backplane design over the last 25 years. He is the founder of LAMSIM Enterprises inc.; providing innovative signal integrity and backplane solutions. He is currently engaged in signal integrity, characterization and modeling of high speed serial links associated with backplane interconnects. He holds two patents and (co)-author of several publications including an award winning DesignCon2009 paper related to via modeling.