Lamsim Enterprises inc.

Backplane Architecture
High Level Design Example

Bert Simonovich

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Jan 24, 2011

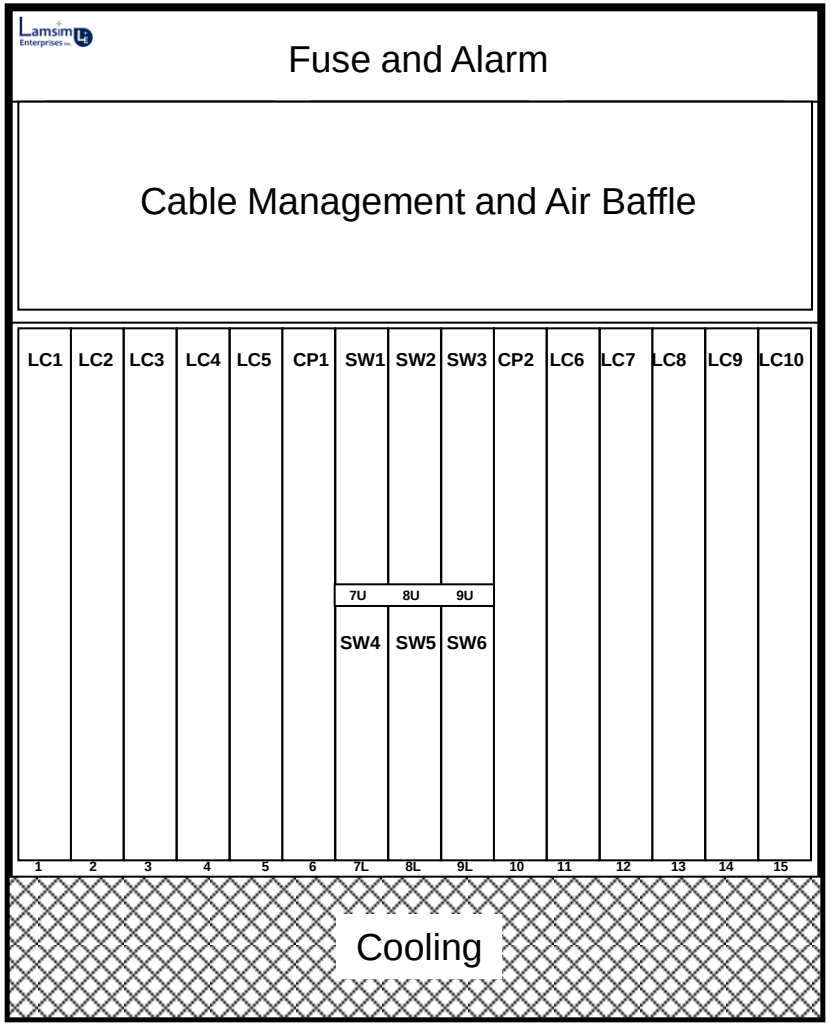
Record of Release

1. Jan 24, 2011: Issue 1.0 - Initial Release.

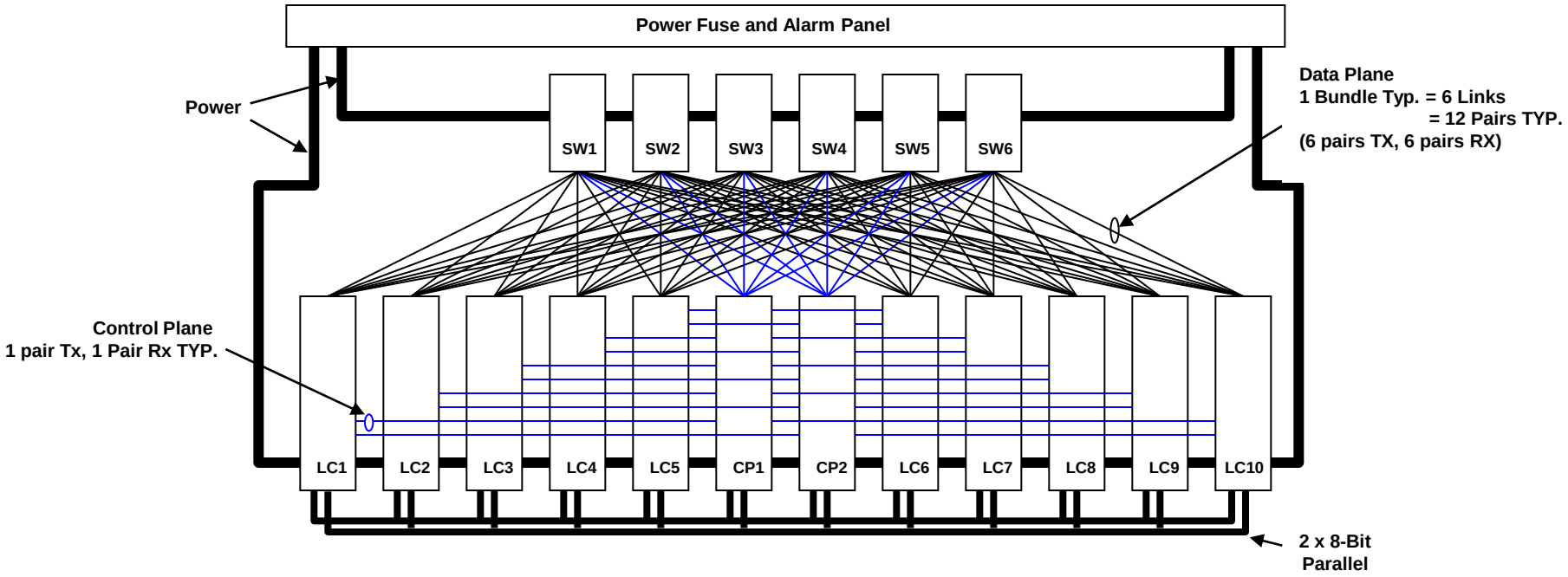
Summary and Caveats

1. This is a sample document intended to demonstrate the principles of Backplane High Level Design Methodology used by LAMSIM Enterprises inc. for a fictitious system architecture.
2. Throughout this document, 1 link = 1Tx&1Rx Pair = 4 Wires.
3. High-speed routing analysis based on TYCO Tin-man connector family.
4. Power distribution and routing analysis not shown since it follows a similar process.
5. Backplane: 18Layer; thickness = 182 mil +/-10%
6. Backplane signal integrity analysis assumes:
   - Plug-in card: 20Layer; Thickness = 114 mil +/-10%
   - 10 GB/s (802.3 10GBaseKR) spec.
   - Backplane via stubs have been counter-bored or back-drilled to minimum 9 mils.
   - Longest Via (150.6 mil); max back-drilled stub (9mil) for Backplane
   - No back-drilling on plug-in cards Shortest Via 3 (23mil); longest stub (75 mil)
   - Plug-in card trace geometry: 4-9-4; Nelco N4000-6
   - Backplane trace geometry 7-9-7; Nelco N4000-13EP

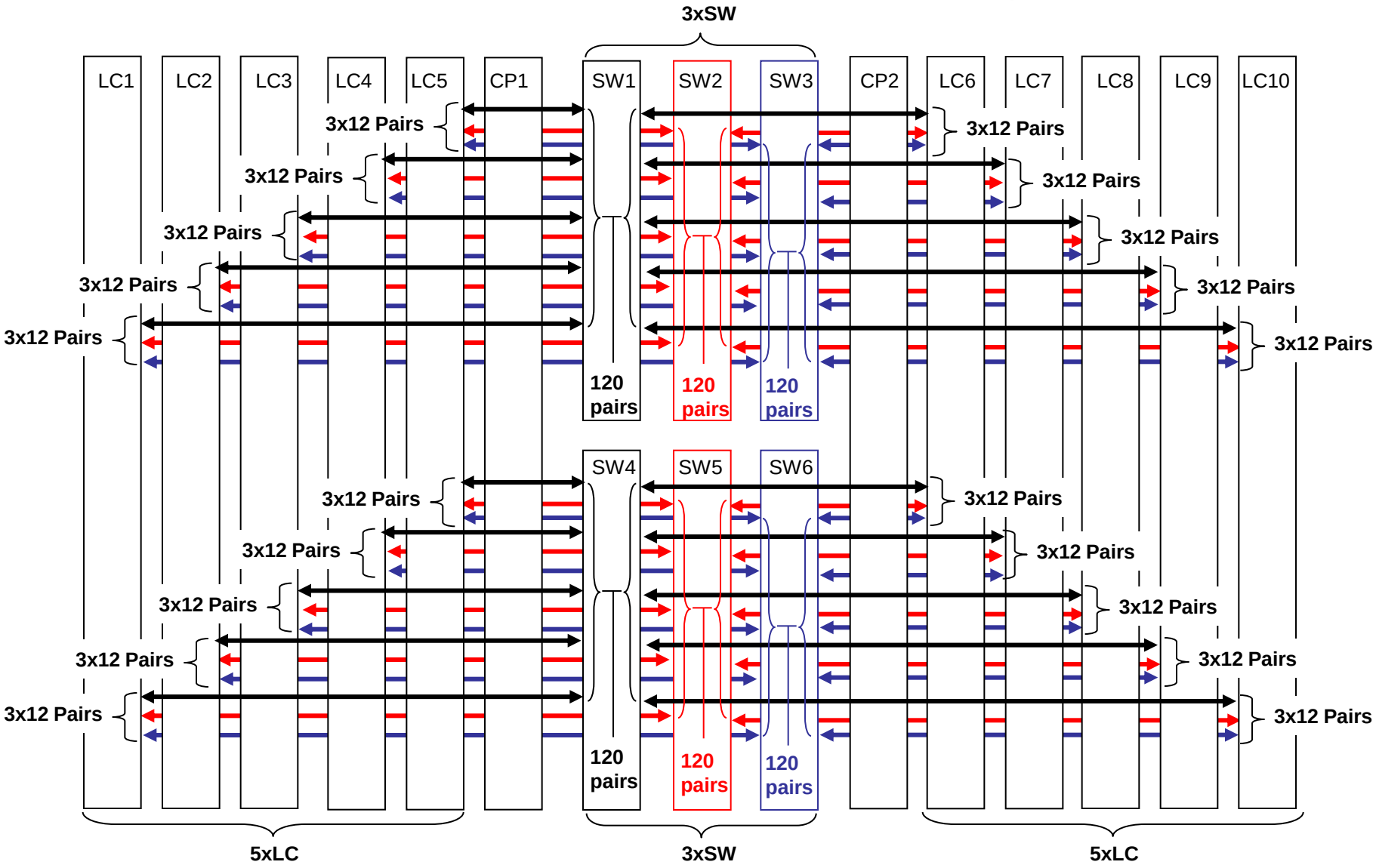
Shelf Slot Numbering and Pack-fill



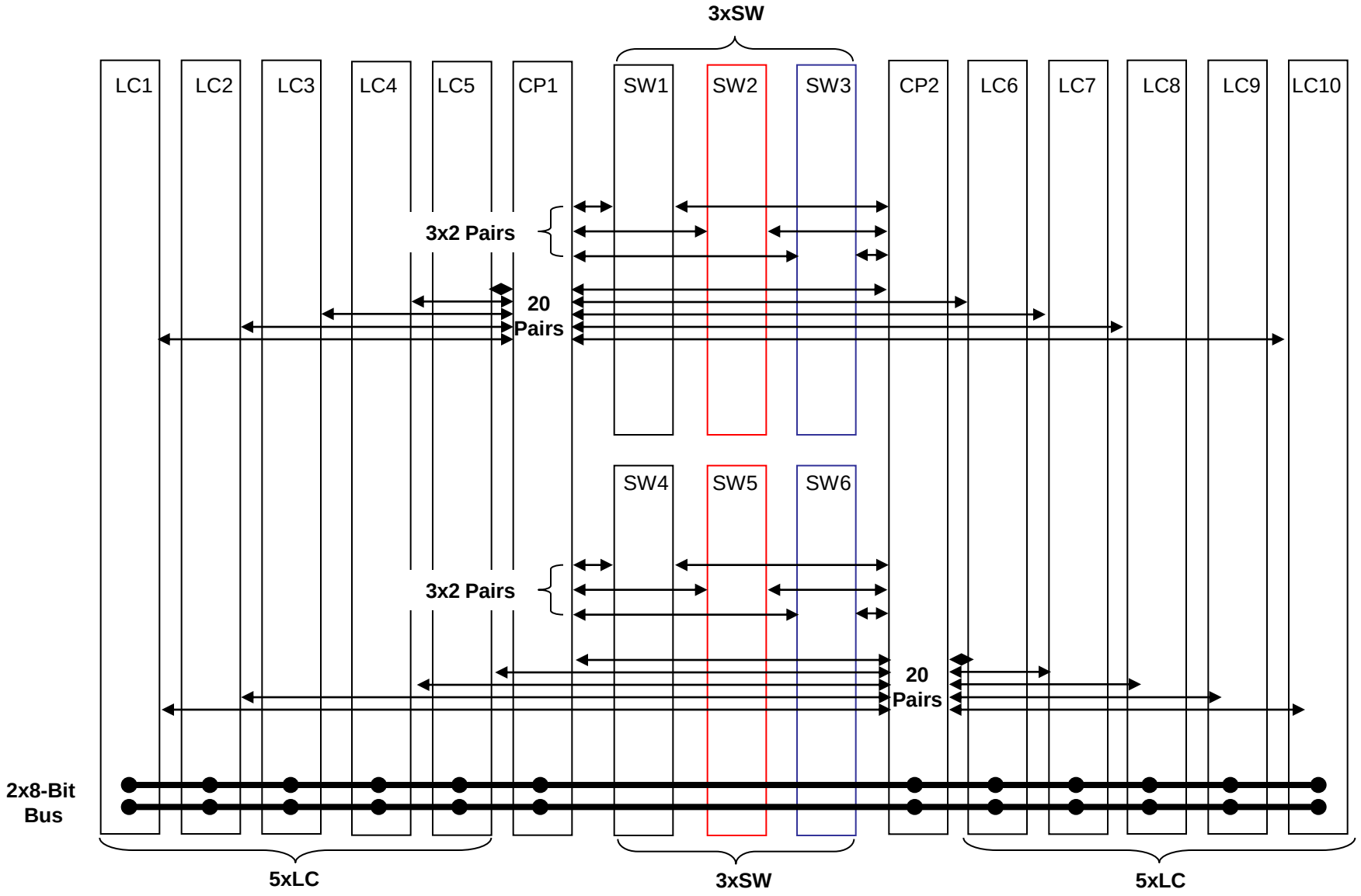
System Block Diagram



System Data Path Block Diagram

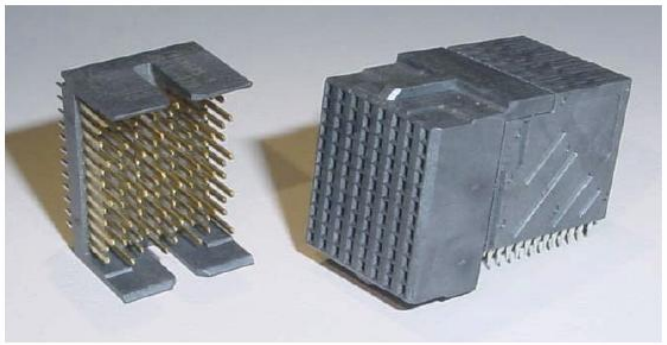


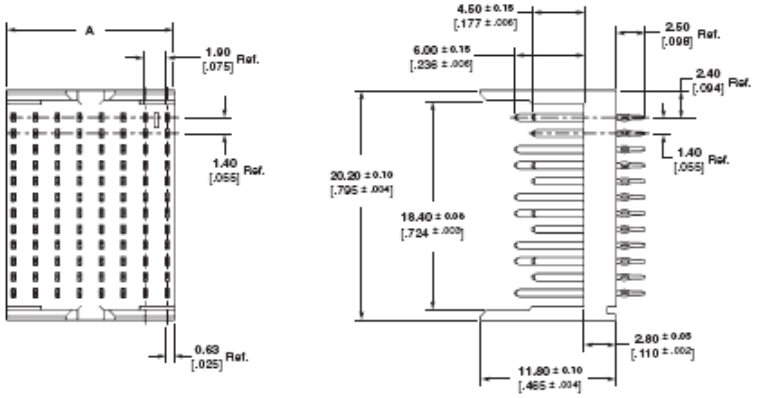
System Control Path Block Diagram - GigE



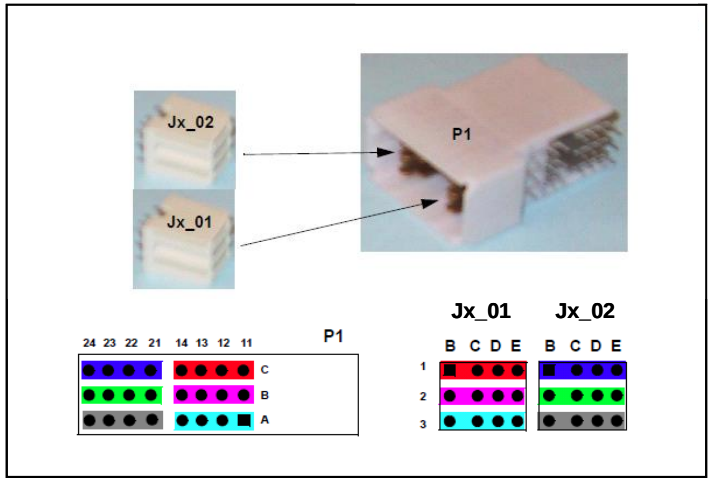
Backplane Connectors

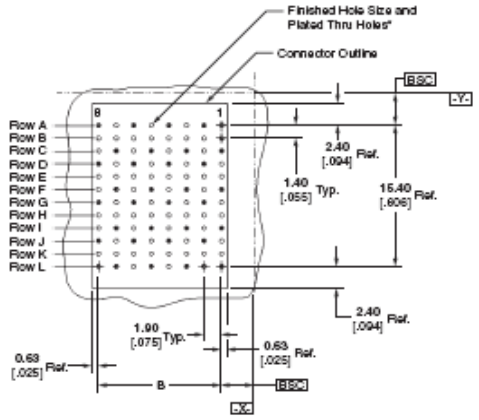
Tyco Tin-Man 4-Pair per Row Connector



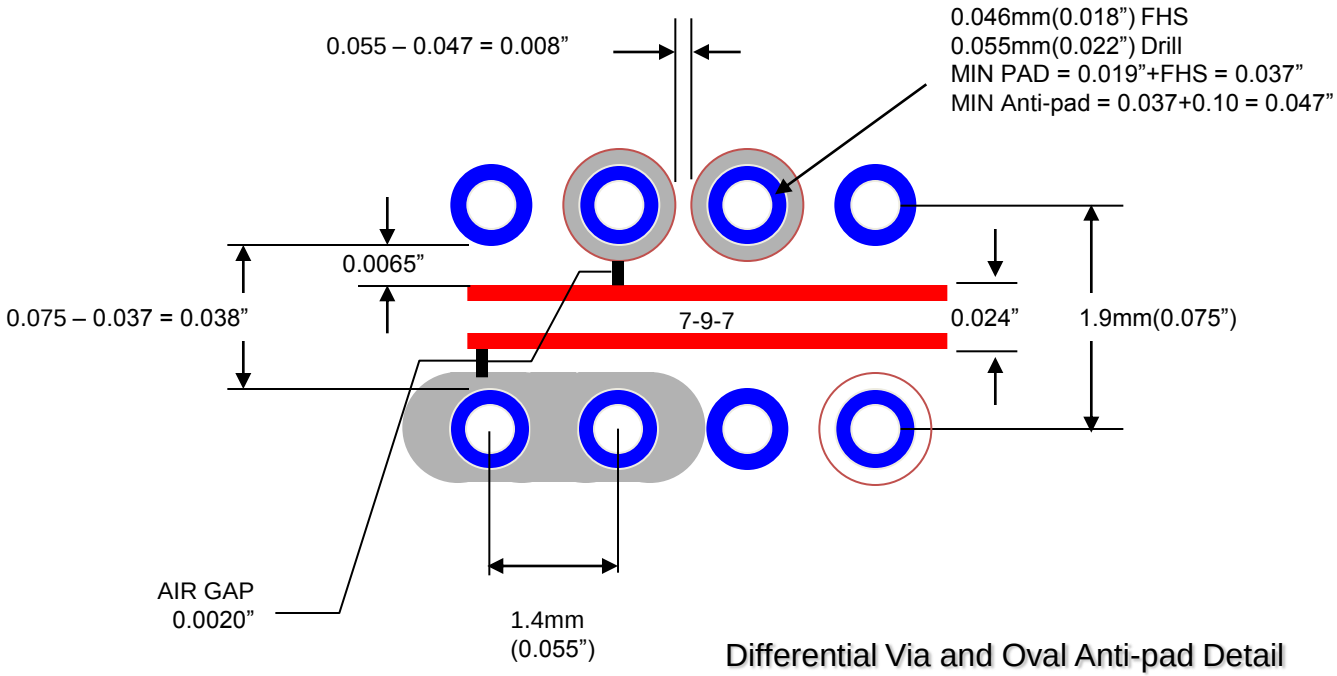


Tyco Power Connector

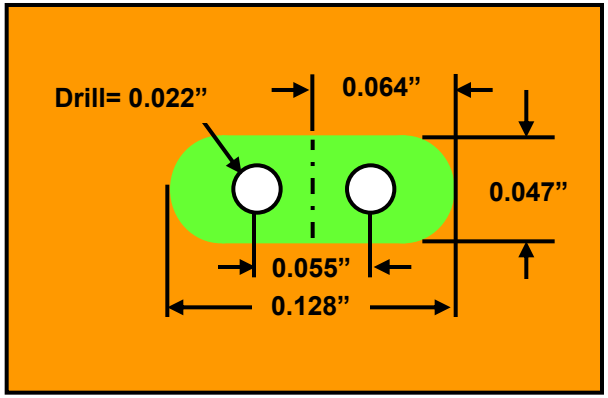




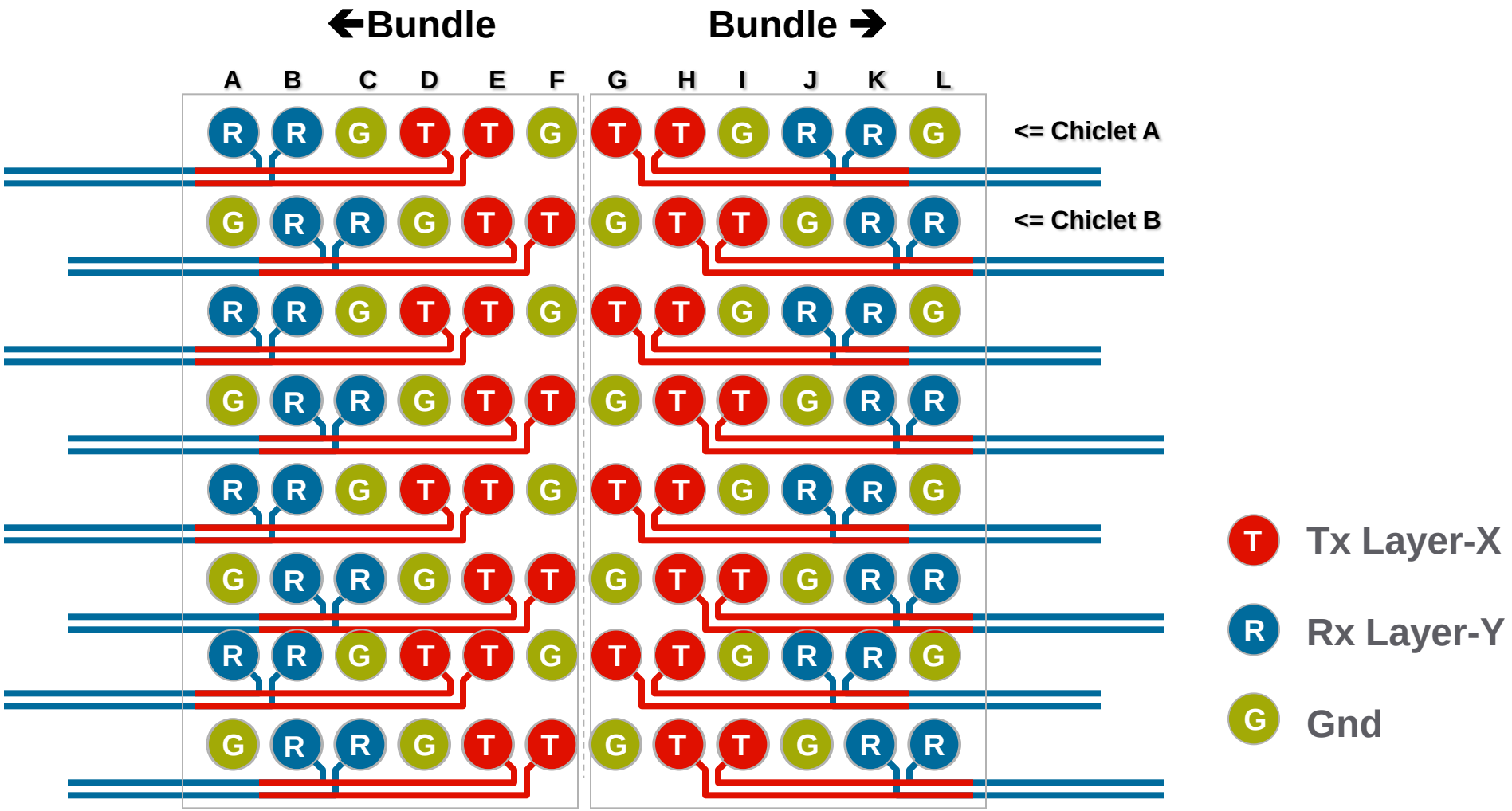
Tin-man Pad/Anti-pad and Routing Channel



Differential Via and Oval Anti-pad Detail



Tin-man Footprint Breakout
Pin Partitioning Preference per Bundle - Switch Card



ETSI (ETS 300 119-4: January 1994)

Dimensions for subracks mounted in miscellaneous racks/cabinets		(NOTE 2)				
H	= height	C	n x 25			
W1	= overall width over flanges	C	535 (NOTE 1)		535	
W2	= width	C	450		500	
W3	= mounting centre distance	A	515 (NOTE 1)		515	
R	= mounting position	C	12,5 + n x 25		12,5 + n x 25	
S	= mounting	A	n x 25		n x 25	
D1	= mounting depth (front)	C	rack 300 deep	rack 600 deep	rack 300 deep	rack 600 deep
			40	75	40	75
D2	= mounting depth (rear)	C	240	470	240	470

NOTE 1: Subracks with dimensions W1 =485 and W3=465 may be fitted into miscellaneous racks (ETS 300 119-3 [4]) by the use of adaptors.

NOTE 2: A = Actual dimension.

Tolerances needed for W3 and S are specified in IEC 917-2-2 (see Annex B).

C = Coordination dimension.

NOTE 3: n = 0, 1, 2, 3....(the value of n can be different for H, R and S).

Definition: A coordination dimension is a reference dimension used to coordinate mechanical interfaces. This is not a manufacturing dimension with a tolerance.

An aperture dimension is a special coordination dimension for a usable space between features.

An actual outside dimension corresponding to a coordination dimension can only decrease.

An actual inside dimension corresponding to an aperture dimension can only increase.

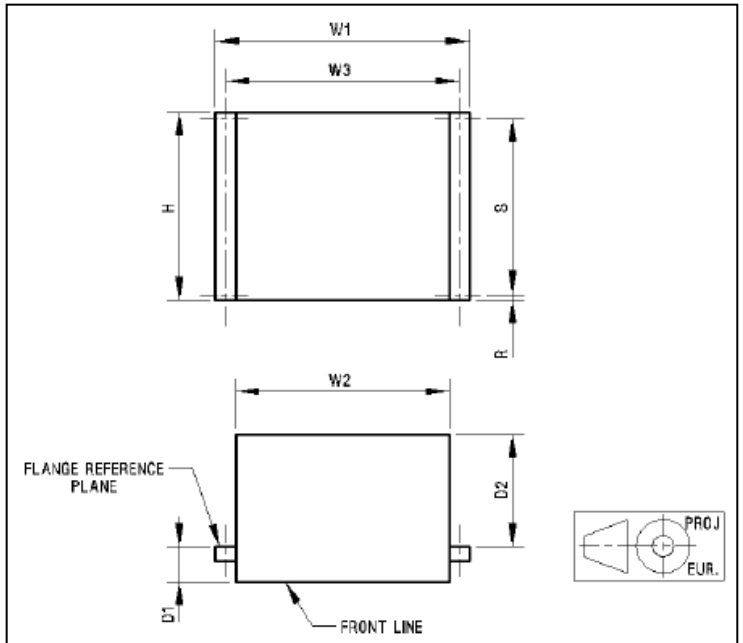
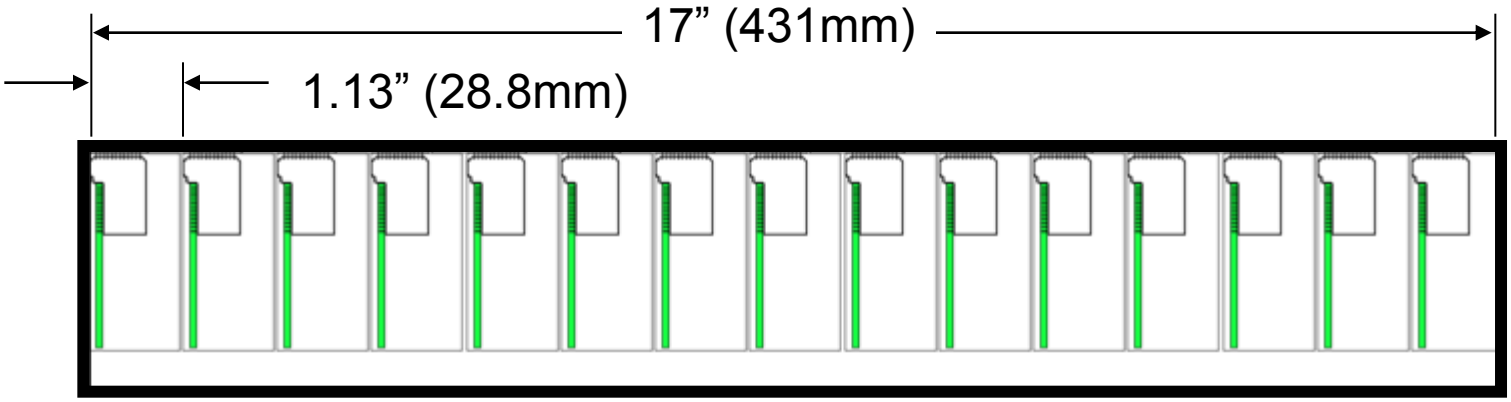


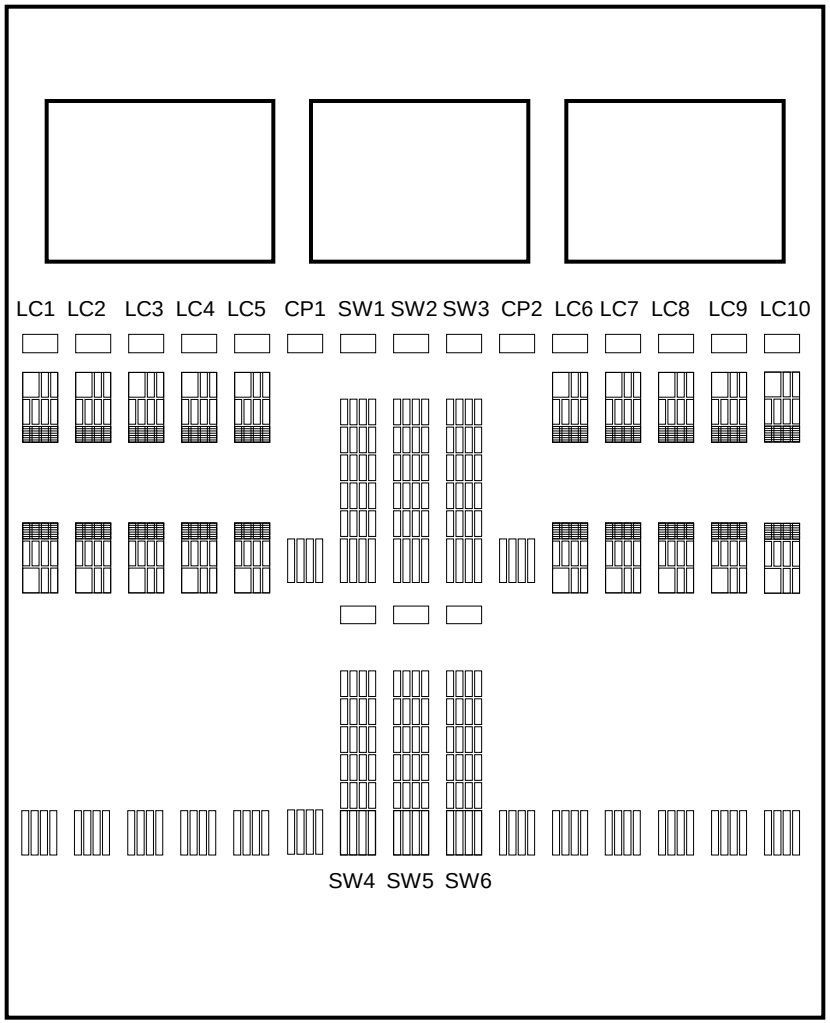
Figure A.1: Subrack

Slot Pitch Determination



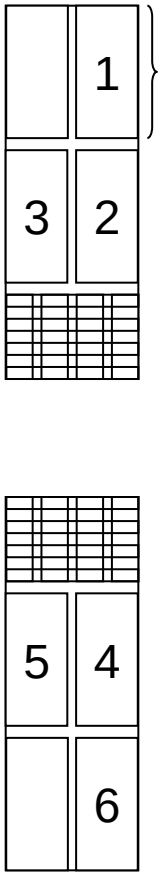
Pitch = 17”/15 cards = 1.13” (28.8mm)

Preliminary Backplane PCB Common Features



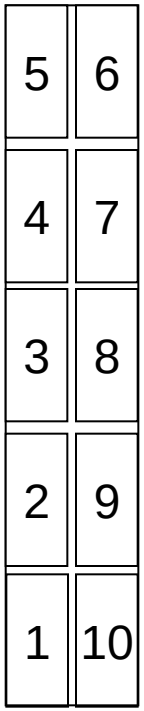
Line Card / Switch Card Link Bundle to Slot Mapping

LC – SW Mapping



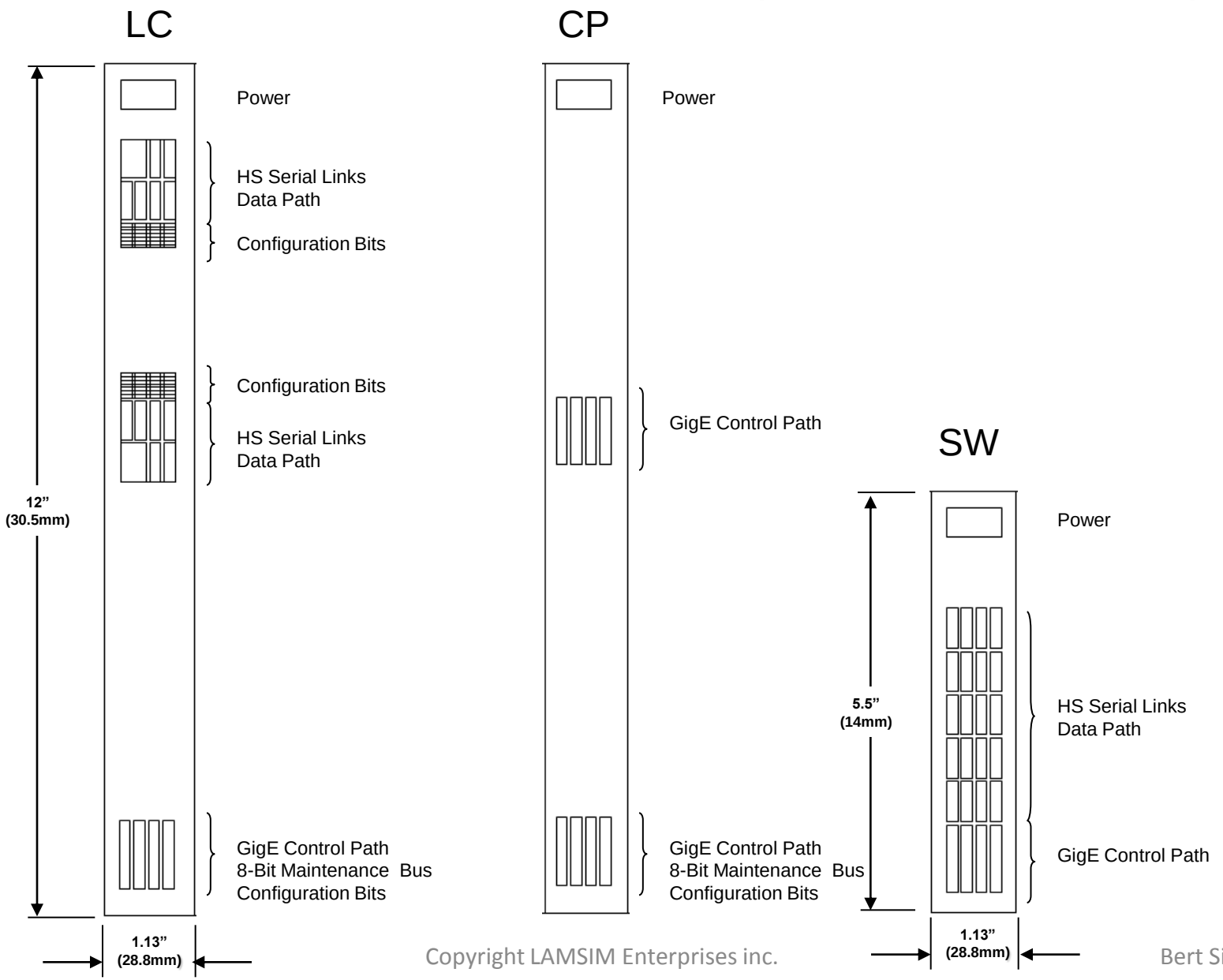
1 Bundle of 6 Tx, 6 Rz Pairs Typ.

SW – LC Mapping



1 Bundle of 6 Tx, 6 Rz Pairs Typ.

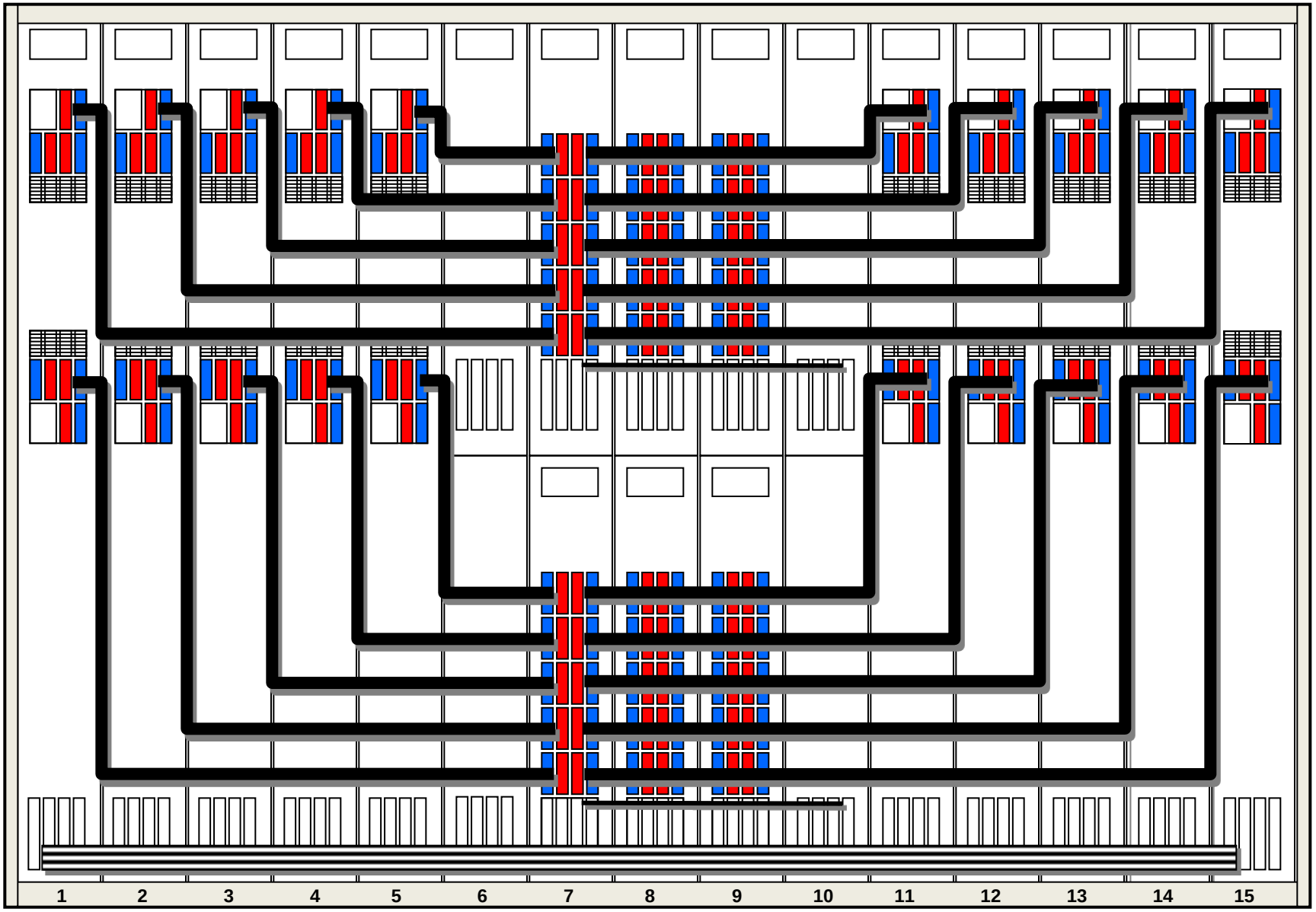
Card Size and Connector Signal Partitioning



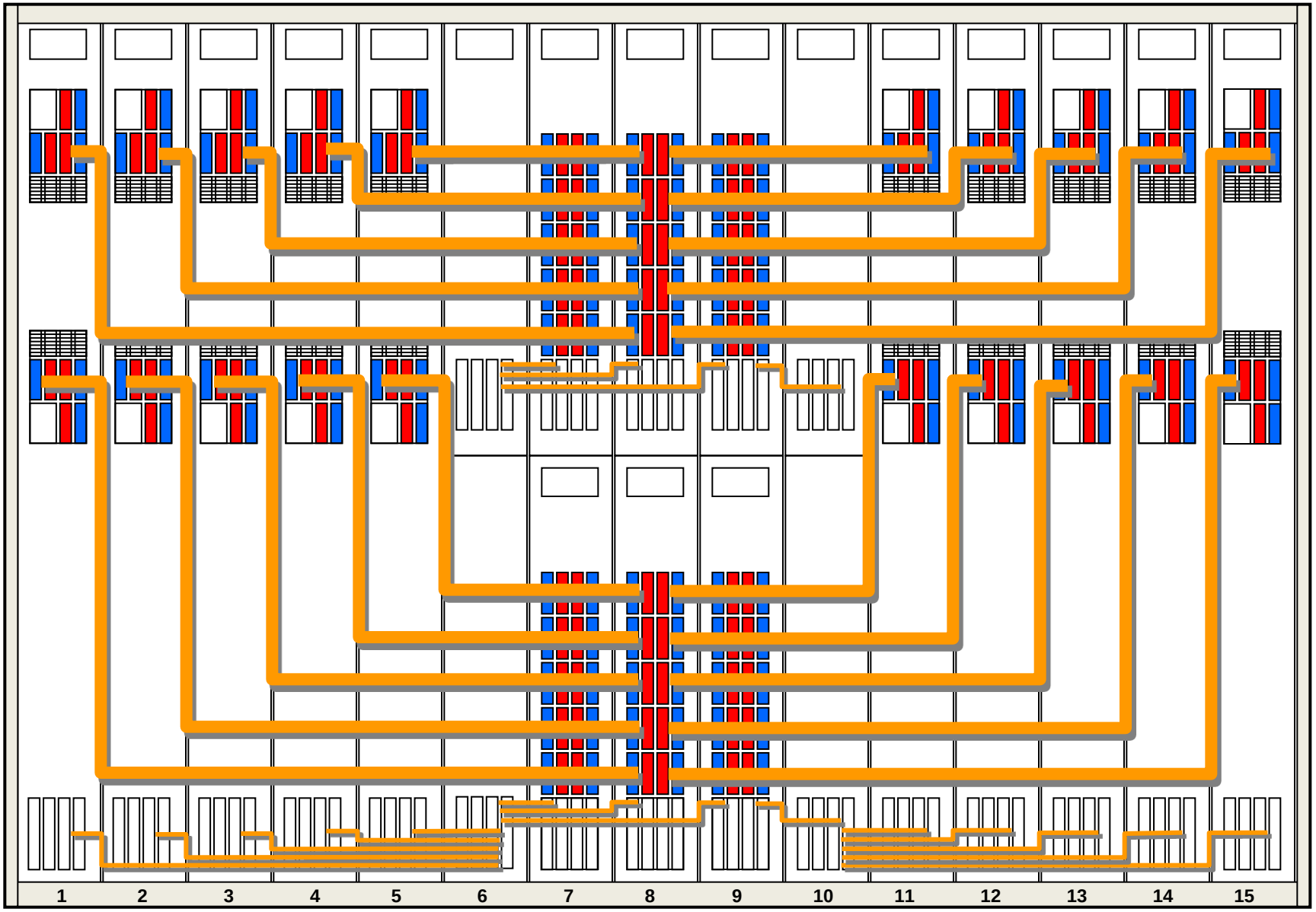
Pin List

	A	B	C	D	E	F	G
1			Circuit Pack				
2	**Function**		**CP**	**LC**	**SW**		
3							
4	HS-Links		0	72	120	pairs	
5	GigE		32	4	4	pairs	
6		subtotal	**32**	**76**	**124**	**pairs**	
7							
8		subtotal	**64**	**152**	**248**	**pins**	
9							
10	Maintenance Bus		16	16	0	pins	
11							
12							
13	Power		24	24	24	pins	
14							
15		**Total**	**104**	**192**	**272**	**pins**	
16							
17							

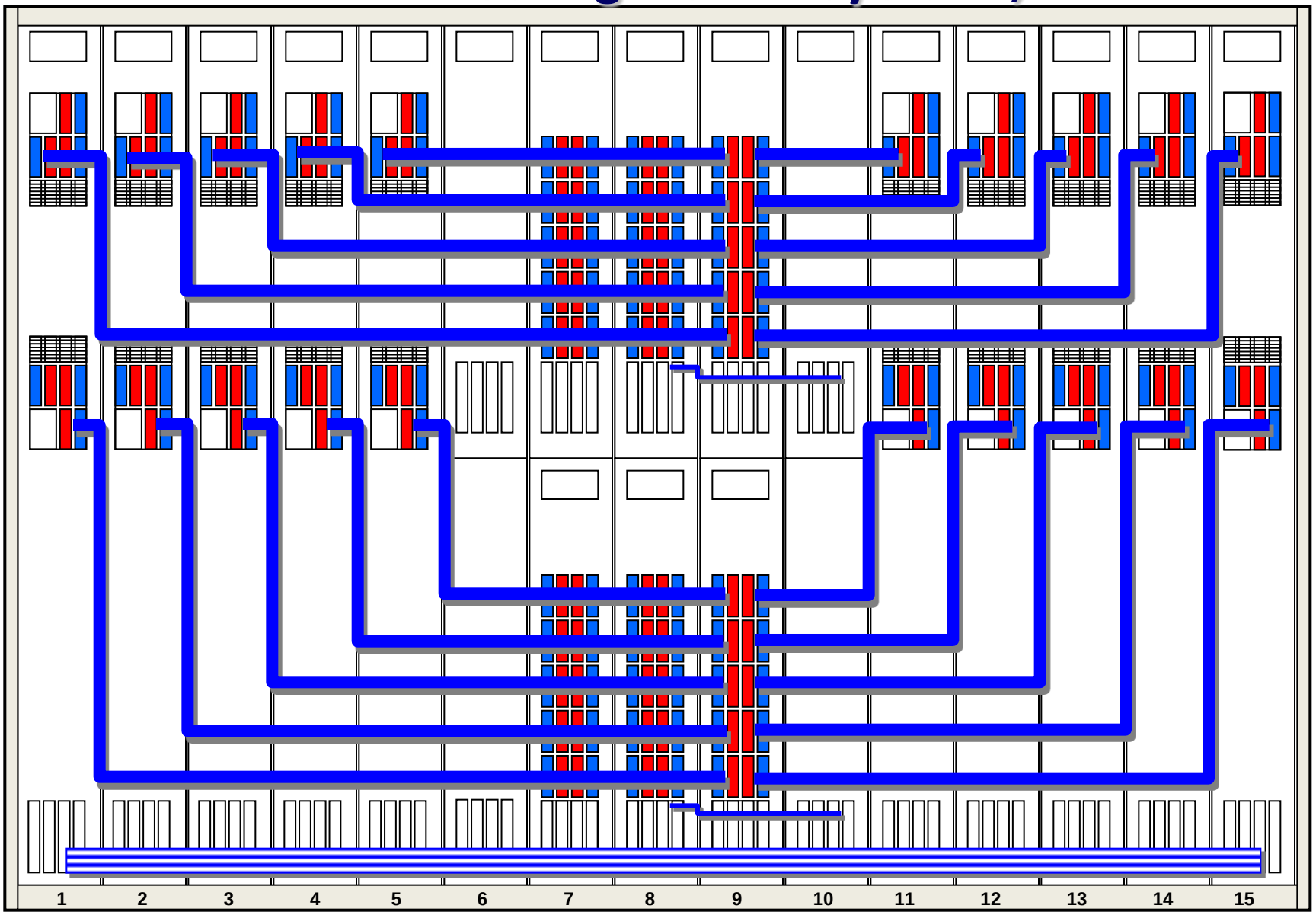
HLD Routing Plan – Layers 7,13



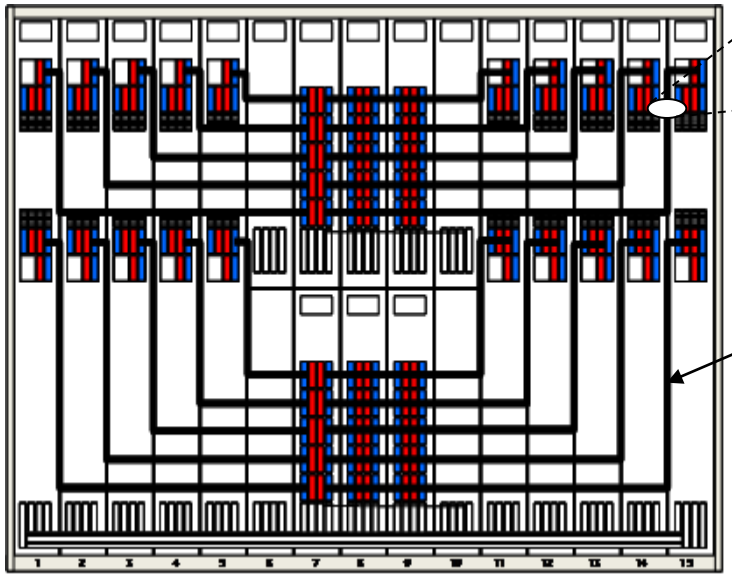
HLD Routing Plan – Layers 9,15

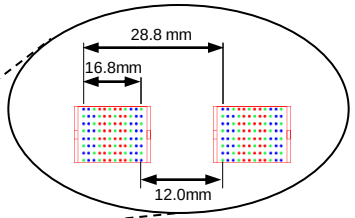


HLD Routing Plan – Layers 11,17



Vertical Routing Channels



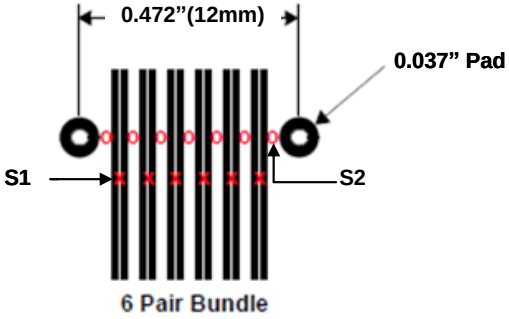


1.13” pitch = 28.8mm
11 pins*1.4mm = 16.8mm
Routing Pitch = 12.0mm
= 0.472”
- Pad Dia. 0.037”

Min Routing Channel= 0.435”

Routing Channel Details

1 Bundle = 6 Tx; 6 Rx Pairs Typ.
= 6 pairs per Sig Layer
= 12 Tracks



6 Pair 5-8-5 geometry	6 Pair 7-9-7 geometry	6 Pair 8-9-8 geometry
12 Tracks * 0.005 = 0.060”	12 Tracks * 0.007 = 0.084”	12 Tracks * 0.008 = 0.096”
6S1 * 0.008 = 0.048”	6S1 * 0.009 = 0.054”	6S1 * 0.009 = 0.054”
7S2 * 0.020 = 0.140”	7S2 * 0.020 = 0.140”	7S2 * 0.020 = 0.140”
Min = 0.248”	Min = 0.278”	Min = 0.290”

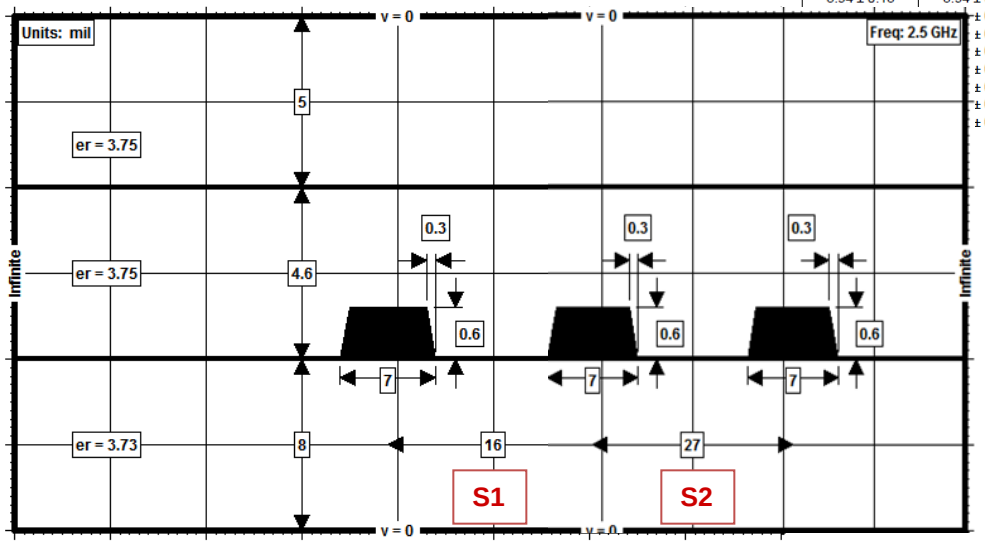
Backplane 7-9-7-20-7-9-7 Differential Pair Geometry

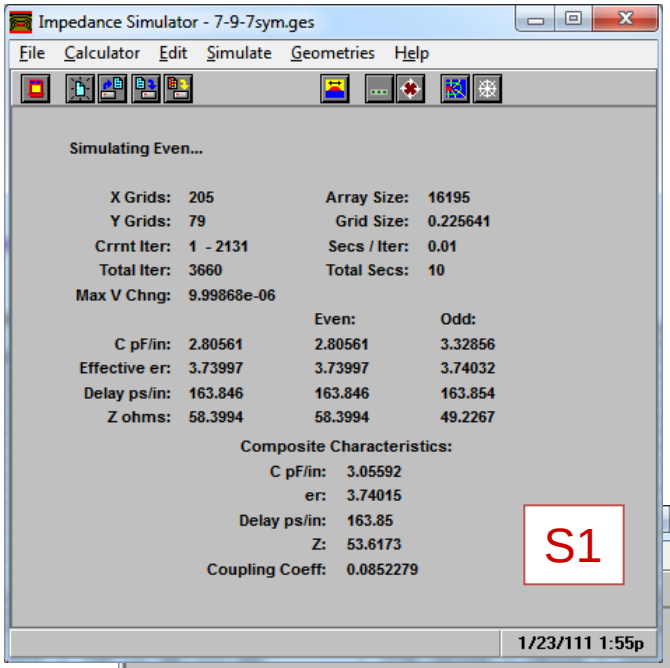
N4000-13EP – Dielectric Properties Table

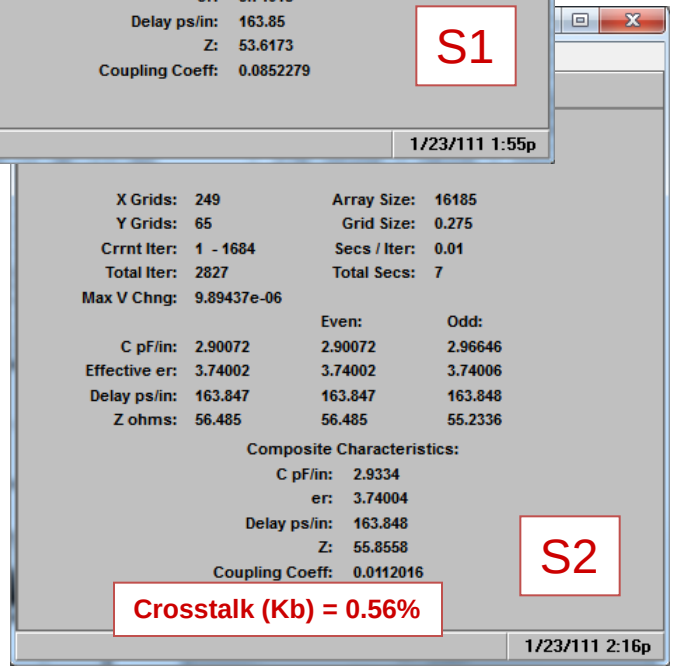
12/18/07

LAMINATE

Thickness	&	Tolerance	Construction	RC%	1 MHz IPC-TM-650 2.5.5.3	1 GHz IPC-TM-650 2.5.5.9	2.5GHz IPC-TM-650 2.5.5.5	10GHz IPC-TM-650 2.5.5.5
0.0020	±	0.0005	1 106	68.3%	3.42 ± 0.11	3.32 ± 0.10	3.31 ± 0.09	3.27 ± 0.10
0.0025	±	0.0005	1 1080	55.2%	3.71 ± 0.14	3.61 ± 0.14	3.56 ± 0.12	3.54 ± 0.13
0.0030	±	0.0005	1 1080	61.2%	3.57 ± 0.10	3.47 ± 0.10	3.44 ± 0.09	3.40 ± 0.09
0.0040	±	0.0005	1 1080 + 1 106	56.9%	3.67 ± 0.09	3.57 ± 0.09	3.52 ± 0.08	3.50 ± 0.08
0.0040	±	0.0005	1 2113	53.8%	3.75 ± 0.10	3.64 ± 0.10	3.59 ± 0.09	3.57 ± 0.09
0.0050	±	0.0007	1 1080 + 1 1080	55.2%	3.71 ± 0.11	3.61 ± 0.10	3.56 ± 0.09	3.54 ± 0.10
0.0050	±	0.0007	1 2116	51.0%	3.82 ± 0.12	3.71 ± 0.12	3.65 ± 0.10	3.64 ± 0.11
0.0050	±	0.0007	1 2113 + 1 106	52.0%	3.80 ± 0.12	3.69 ± 0.11	3.63 ± 0.10	3.61 ± 0.11
0.0055	±	0.0007	2 1080	58.4%	3.63 ± 0.09	3.53 ± 0.08	3.49 ± 0.08	3.46 ± 0.08
0.0060	±	0.0007	2 2113	42.7%	4.07 ± 0.14	3.95 ± 0.13	3.87 ± 0.12	3.86 ± 0.12
0.0060	±	0.0007	1 2116 + 1 106	50.0%	3.85 ± 0.11	3.74 ± 0.10	3.68 ± 0.09	3.66 ± 0.10
0.0060	±	0.0007	1 1080 + 1 2113	51.4%	3.81 ± 0.10	3.70 ± 0.10	3.64 ± 0.09	3.63 ± 0.09
0.0060	±	0.0007	1 106 + 1 2116	50.0%	3.85 ± 0.11	3.74 ± 0.10	3.68 ± 0.09	3.66 ± 0.10
0.0070	±	0.001	2 2113	48.8%	3.88 ± 0.13	3.77 ± 0.13	3.71 ± 0.11	3.69 ± 0.12
0.0075	±	0.001	1 7628	41.0%	4.13 ± 0.16	4.01 ± 0.16	3.92 ± 0.14	3.91 ± 0.15
0.0080	±	0.001	2 2116	42.3%	4.08 ± 0.15	3.96 ± 0.14	3.88 ± 0.13	3.87 ± 0.13
0.0080	±	0.001	1 2116 + 1 2113	47.8%	3.91 ± 0.12	3.80 ± 0.12	3.73 ± 0.11	3.72 ± 0.11
0.0090	±	0.001	1 2116 + 1 2116	47.0%	3.93 ± 0.11	3.82 ± 0.11	3.75 ± 0.10	3.74 ± 0.10
0.0100	±	0.001	2 2116	51.0%	3.82 ± 0.09	3.71 ± 0.09	3.65 ± 0.08	3.64 ± 0.08
0.0100	±	0.001	1 7628 + 1 1080	44.3%	4.02 ± 0.11	3.90 ± 0.11	3.82 ± 0.10	3.81 ± 0.10
0.0110	±	0.001	2 106 + 1 7628	47.7%	3.91 ± 0.09	3.80 ± 0.09	3.73 ± 0.08	3.72 ± 0.08
							3.81 ± 0.12	3.80 ± 0.12
							3.94 ± 0.13	3.94 ± 0.13







PCB Stack-up and Counter-bore Details

From: Bert Simonovich

Layer	Thk.	Layer Type	Layer Definition		Edge coupled diff Design: Width	Edge coupled diff Design: Imped
	0.7	mask				
L01	2.1	.5oz foil &plate	PRI			
	9.0	prepreg				
L02	2.8		BRETA			
	5.0	2/2core				
L03	2.8		-48A			
	9.0	prepreg				
L04	2.8		-48B			
	5.0	2/2core				
L05	2.8		BRETB			
	9.0	prepreg				
L06			gnd			
	8.0	.5/.5core				
L07	0.6		sig	Rx	7-9-7	100.0Ω
	9.0	prepreg				
L08	0.6		gnd			
	8.0	.5/.5core				
L09	0.6		sig	Rx	7-9-7	100.0Ω
	9.0	prepreg				
L10	0.6		gnd			
	8.0	.5/.5core				
L11	0.6		sig	Rx	7-9-7	100.0Ω
	9.0	prepreg				
L12	0.6		gnd			
	8.0	.5/.5core				
L13	0.6		sig	Tx	7-9-7	100.0Ω
	9.0	prepreg				
L14	0.6		gnd			
	8.0	.5/.5core				
L15	0.6		sig	Tx	7-9-7	100.0Ω
	9.0	prepreg				
L16	0.6		gnd			
	8.0	.5/.5core				
L17	0.6		sig	Tx	7-9-7	100.0Ω
	9.0	.5/.5core				
L18	2.1	.5oz foil &plate	gnd			
	0.7	mask				

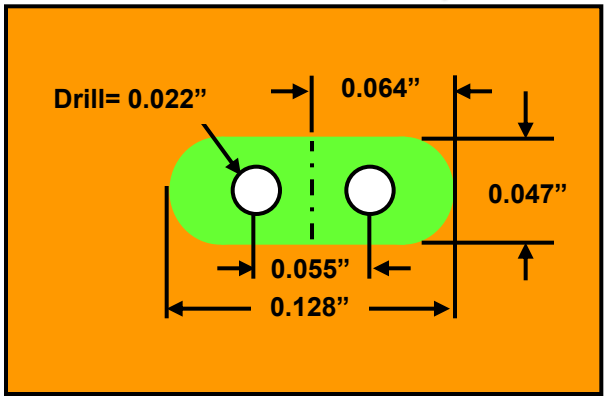
	Tx Vias: C-bor Via 6	Tx Vias: C-bor Via 5	Tx Vias: C-bor Via 4	Rx Vias: C-bor Via 3	Rx Vias: C-bor Via 2	Rx Vias: C-bor Via 1	MIN Depth
Via Len	150.60	132.40	114.20	96.00	77.80	59.60	59.60
Stub	9.00	9.00	9.00	9.00	9.00	9.00	

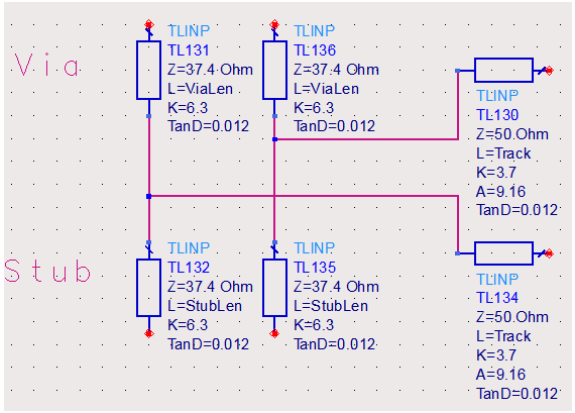
Total:	156.8	Finish thickness Glass to Glass +-10%
	161.0	Finish thickness over plating +-10%
	162.4	Overall Thickness incl. Mask
A.R.	7.3	Aspect Ratio

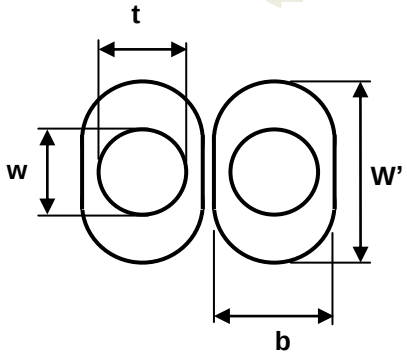
FOR DESIGN REFERENCE ONLY - TO BE CONFIRMED BY MFG PRIOR TO FABRICATION - Dielectric thicknesses and line widths are for reference only and may be modified to achieve specified impedances.

Tin-man Backplane Via Impedance and Model

Diff Via and Anti-pad







s = 0.055”
b = 0.064”
W’ = 0.047”
r = ½(0.022”)
w = 0.022”
t = 0.022”
Dk_{avg}= 3.74

$$Zvia \cong \frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r}+\sqrt{\left(\frac{s}{2r}\right)^2-1}\right)\times\ln\left(\frac{W'+b}{w+t}\right)}$$

$$Dkeff \cong Dkavg \times \frac{\ln\left(\frac{s}{2r}+\sqrt{\left(\frac{s}{2r}\right)^2-1}\right)}{\ln\left(\frac{W'+b}{w+t}\right)}$$

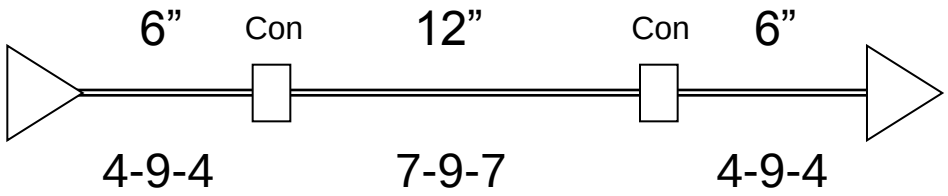
$$\cong \frac{60}{\sqrt{3.74}} \times \sqrt{\ln\left(\frac{0.055}{0.022}+\sqrt{\left(\frac{0.055}{0.022}\right)^2-1}\right)\times\ln\left(\frac{0.047+0.064}{0.022+0.022}\right)}$$

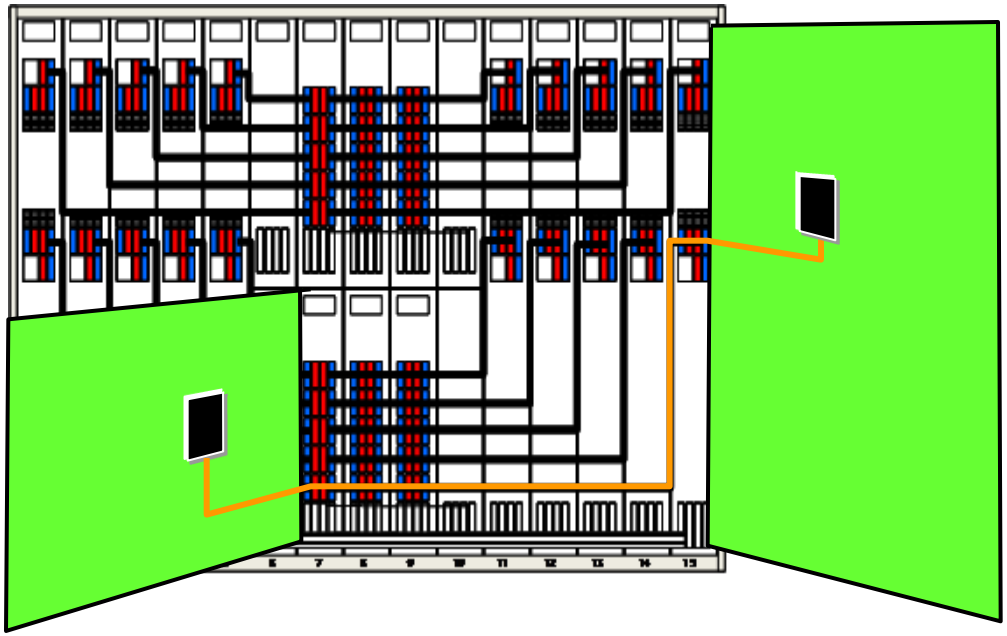
$$\cong 3.74 \times \frac{\ln\left(\frac{0.055}{0.022}+\sqrt{\left(\frac{0.055}{0.022}\right)^2-1}\right)}{\ln\left(\frac{0.047+0.064}{0.022+0.022}\right)}$$

$$\boxed{Zvia \cong 37.4\Omega}$$

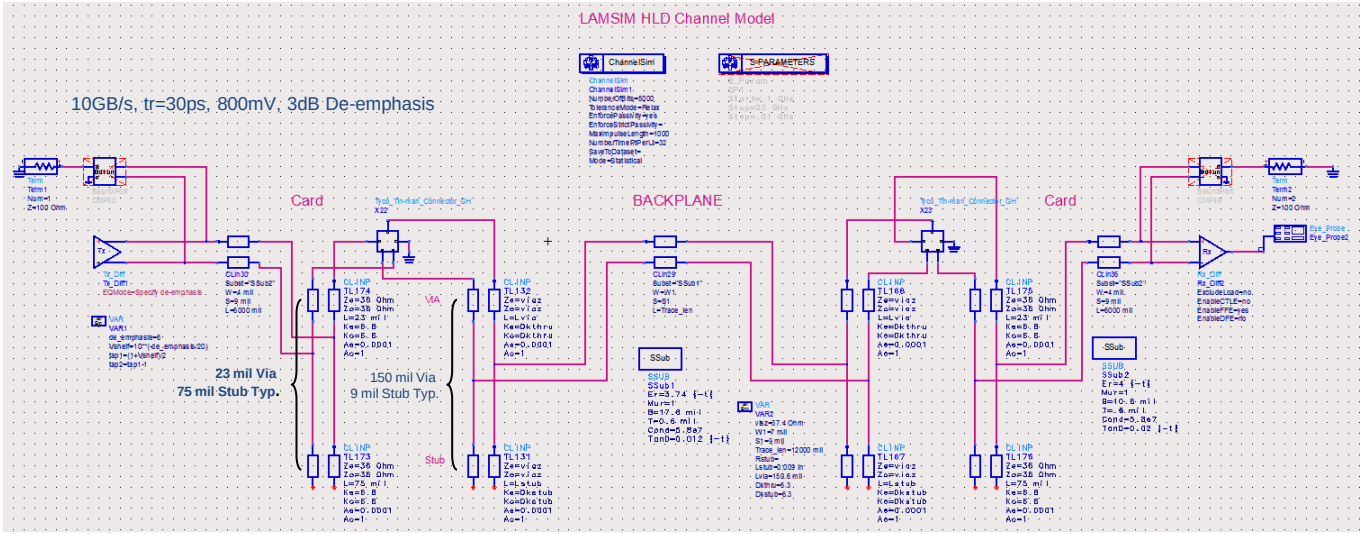
$$\boxed{Dkeff \cong 6.33}$$

Signal Integrity Ref Topology





Agilent ADS Channel Modeling and Simulation 10GBASEKR



Eye @ 10^{-16} BER

Height = 229mV

Width = 50 ps