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Practical Model of Conductor Surface Roughness Using Cubic Closepacking of Equal Spheres

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Abstract

In the GB/s regime, accurate modeling of conductor losses is a precursor to successful high-speed serial link designs. In this paper, a practical method for modeling conductor surface roughness is presented. Obtaining the roughness parameters solely from manufacturers' data sheets, conductor loss can now be accurately predicted from first principles. By using a cubic close-packing of equal spheres model, the radius of the spheres and area of the multi-sphere tiled base are determined then applied to the Huray "snowball" model. A case study using FR408HR material with reverse treated copper foil is used to validate the model's accuracy to 50GHz.

Author(s) Biography

Lambert (Bert) Simonovich graduated in 1976 from Mohawk College of Applied Arts and Technology, Hamilton, Ontario Canada, as an Electronic Engineering Technologist. Over a 32-year career, working at Bell Northern Research/Nortel, in Ottawa, Canada, he helped pioneer several advanced technology solutions into products. He has held a variety of engineering, research and development positions, eventually specializing in high-speed signal integrity and backplane architectures. After leaving Nortel in 2009, he founded Lamsim Enterprises Inc., where he continues to provide innovative signal integrity and backplane solutions as a consultant. He has also authored and coauthored several publications which are posted on his web site at <u>www.lamsimenterprises.com</u>. His current research interests include: high-speed signal/power integrity, modeling and characterization of high-speed serial link architectures.

Introduction

At high frequencies, the conductor and dielectric losses lead to dispersion of the transmitted signal. The total loss of the transmission path is the sum of dielectric and conductor losses. Predicting total loss using smooth copper and published loss tangent values is no longer adequate in the 10-plus GB/s regime.

The traditional Hammerstad-Jensen model has been used for decades to account for increased losses. It assumes a two dimensional, triangular corrugated surface to represent the conductor roughness. This model is based solely on a mathematical fit to power loss data published by S.P. Morgan in 1949. The roughness correction coefficient is determined by a simple equation. All that is required is the RMS surface roughness parameter as published in manufacturers' data sheets. Although it is a simple model and easy to use, there is no theoretical basis to support it. It is only accurate up to approximately 3-15 GHz, depending on severity of roughness.

The Huray model is based on a collection of spheres, resembling "snowballs", stacked in a pyramidal geometry. If the size and number of spheres are known, a roughness correction factor can be analytically solved through a simple equation. The problem has always been getting the necessary parameters, usually through sophisticated scanning electron microscope (SEM) measurements, and fitting them with empirical data through simulation.

In a DesignCon2013 paper [7] the authors compare both models, and discussed why it was not practical to take information directly from manufacturers' data sheets, since the information is not always in a format that immediately translates into mathematical parameters for commercial simulators. Instead they relied on measured response data from a test board to fit parameters associated with conductor and dielectric losses. They then go on to use the extracted parameters in circuit simulators to create scalable transmission line models for any interconnect.

Obtaining good measured data requires considerable effort. First the PCB must be properly designed to facilitate accurate extraction of S-parameter data. Next expensive test equipment and skill is required in the measurement and de-embedding of the fixture. Finally, considerable expertise and know-how is needed to tune the parameters such that the final model fits both insertion loss and phase. All this adds up to increased time and dollars, and is beyond the scope and resources of most companies.

The motivations for this research work were to follow-up on the previous work [1], and to test the accuracy of an alternate cubic close-packing equal spheres (CCPES) model solely from manufacturers' data sheets.

The main difference between the two models is in their stacking arrangement and the total number of spheres used. The HCPES model described in [1] was founded on 11 stacked spheres over a hexagonal base, while the CCPES model is based on 14 stacked spheres over a square base. The CCPES model proved to be just as accurate but with simpler equations.

When the sphere radius and area parameters from the CCPES model were analytically applied to the Huray model, its accuracy was compared to experimental data through a case study using FR408HR/RTF material up to 50GHz. This paper presents the results of that study.

Background

The total loss of a printed circuit board (PCB) transmission line, as a function of frequency, is the sum of dielectric and conductor loss as shown by example in Figure 1. The difference between the simulated total loss and measured loss is due to conductor surface roughness.

In this example, the foil type used was very low profile (VLP). Although it is a relatively smooth foil, compared to the standard foil, failure to model roughness effects for designs running at 25GB/s can ruin you day.



Figure 1 Comparisons of measured insertion loss (red) vs simulated (blue) insertion loss of conductor. Modeled and simulated with Keysight EEsof EDA ADS software [14].

Figure 2 shows eye diagrams at 25 Gb/s for measured loss with rough copper (left) and total loss of smooth copper (right). With just -3.2dB delta in insertion loss at 12.5 GHz, there is half the eye height opening with rough copper.



Figure 2 Simulated eyes of measured loss with rough copper (left) vs smooth copper (right) at 25 Gb/s. Modeled and simulated with Keysight EEsof EDA ADS software [14].

In printed circuit (PCB) construction there is no such thing as a perfectly smooth conductor surface. There is always some degree of roughness that promotes adhesion to the dielectric material. Unfortunately this roughness also contributes to additional conductor loss.

Electro-deposited (ED) copper is widely used in the PCB industry. A finished sheet of ED copper foil has a matte side and drum side. The drum side is always smoother than the matte side.

The matte side is usually attached to the core laminate. For high frequency boards, sometimes the drum side of the foil is laminated to the core. In this case it is referred to as reversed treated foil (RTF).

Various foil manufacturers offer ED copper foils with varying degrees of roughness. Each supplier tends to market their product with their own brand name. Presently, there are three distinct classes of copper foil roughness:

- Standard
- Very-low profile (VLP)
- Ultra-low profile (ULP) or profile free (PF)

Standard is the most common profile, and has no minimum or maximum IPC roughness spec. VLP roughness is typically any foil with a roughness of less than 5.2 microns, while ULP is a newer class of copper with roughness less than 2 microns max. Since there is no official IPC spec as yet, other names like HVLP, ULP, PF, VSP or eVLP are often used.

Profilometers are often used to quantify the roughness tooth profile of electro-deposited copper. Tooth profiles are typically reported in terms of 10-point mean roughness (R_z) for both sides, but sometimes the drum side reports average roughness (R_a) in manufacturers' data sheets. Some manufacturers may also report RMS roughness (R_q).

Modeling Roughness

Alternating current (AC) causes conductor loss to increase in proportion to the square root of frequency. This is due to the redistribution of current towards the outer edges caused by skin-effect. The resulting skin-depth (δ) is the effective thickness where the current flows around the perimeter and is a function of frequency.

Skin-depth at a particular frequency is determined by:

Equation 1

$$\delta = \sqrt{\frac{1}{\pi f \,\mu_0 \sigma}}$$

Where:

 δ = skin-depth in meters;

f = sine-wave frequency in Hz;

 μ_0 = permeability of free space =1.256E-6 Wb/A-m;

 σ = conductivity in S/m. For annealed copper σ = 5.80E7 S/m.

Several modeling methods were developed over the years to determine a roughness correction factor (K_{SR}). When multiplicatively applied to the smooth conductor attenuation (α_{smooth}), the attenuation due to roughness (α_{rough}) can be determined by:

Equation 2

 $\alpha_{rough} = K_{SR} \alpha_{smooth}$

Hammerstad-Jensen Model

The most popular method, for years, has been the Hammerstad and Jensen (H&J) model, based on work done in 1949 by S. P. Morgan. The H&J roughness correction factor (K_{HJ}), at a particular frequency, is solely based on a mathematical fit to S. P. Morgan's power loss data and is determined by [2]:

Equation 3

$$K_{HJ} = 1 + \frac{2}{\pi} \arctan\left(1.4\left(\frac{\Delta}{\delta}\right)^2\right)$$

Where:

 K_{HJ} = H&J roughness correction factor;

 $\Delta = RMS$ tooth height in meters;

 $\delta =$ skin depth in meters.

The model has correlated well for microstrip geometries up to about 15 GHz, for surface roughness of less than 2 μ m RMS. However, it proved less accurate for frequencies above about 5GHz for very rough copper [3].

Huray Model

In recent years, the Huray model [4] has gained popularity due to the continually increasing data rate's need for better modeling accuracy. The model is based on a non-uniform distribution of spherical shapes resembling "snowballs" and stacked together forming a pyramidal geometry, as shown by the SEM photo in Figure 3.



Figure 3 SEM photograph of electrodeposited copper nodules on a matte surface resembling "snowballs" on top of heat treated base foil. Photo credit Oak-Mitsui.

By applying electromagnetic wave analysis, the superposition of the sphere losses can be used to determine the total loss of the structure. Since the losses are proportional to the surface area of the roughness profile, an accurate estimation of a roughness correction factor (K_{SRH}) can be analytically solved by [7]:

Equation 4

$$K_{SRH}(f) = \frac{A_{matte}}{A_{flat}} + \frac{3}{2} \sum_{i=1}^{j} \frac{\left(\frac{N_i \times 4\pi a_i^2}{A_{flat}}\right)}{\left(1 + \frac{\delta(f)}{a_i} + \frac{\delta^2(f)}{2a_i^2}\right)}$$

Where:

 K_{SRH} (f) = roughness correction factor, as a function of frequency, due to surface roughness based on the Huray model;

 $\frac{A_{matte}}{A_{flat}}$ = relative area of the matte base compared to a flat surface;

 a_i = radius of the copper sphere (snowball) of the i^{th} size, in meters;

 $\frac{N_i}{A_{flat}}$ = number of copper spheres of the *i*th size per unit flat area in sq. meters;

 δ (*f*) = skin-depth, as a function of frequency, in meters.

CCPES Model

Using the concept of cubic close-packing of equal spheres, the radius of the spheres (a_i) and tile area (A_{flat}) parameters for the Huray model can now be determined solely by the roughness parameters published in manufacturers' data sheets.

Why is this important? Well, as Eric Bogatin often says, "*Sometimes an OK answer NOW is more important than a good answer late*". Having a method to accurately predict loss from data sheets alone rather than go through a design feedback method, described in [7] can save an enormous amount of time and money, especially at the front end of a design cycle when one is exploring many engineering design options.

Another reason is that it gives a sense of intuition on what to expect with measurements, or sanitize simulation results from commercial modeling tools to help determine root cause of any differences. It is always prudent to have alternate ways to verify results from design tools.

Recalling that conductor losses are proportional to the surface area of the roughness profile, the CCPES model can be used to optimally represent the surface roughness. As illustrated in Figure 4, there are three rows of spheres stacked on a square tile base. Nine spheres are on the first row, four spheres in the middle row, and one sphere on top.



Figure 4 CCPES model showing a stack of 14 uniform size spheres (left). Top and front views (right) shows the area (A_{flat}) of base, height (H_{RMS}) and radius of sphere (r).

Because the CCPES model assumes the ratio of $A_{matte}/A_{flat} = 1$, and there are 14 spheres, Equation 4 can be simplified to:

Equation 5

$$K_{SR}(f) = 1 + 84 \left(\frac{\left(\frac{\pi r^2}{A_{flat}}\right)}{\left(1 + \frac{\delta(f)}{r} + \frac{\delta^2(f)}{2r^2}\right)} \right)$$

Where:

 $K_{SR}(f)$ = roughness correction factor, as a function of frequency, due to surface roughness based on the CCPES model;

r = sphere radius in meters; $\delta(f) =$ skin-depth, as a function of frequency in meters;

 A_{flat} = area of square tile base surrounding the 9 base spheres in sq. meters.

As shown in Figure 5, there are 5 square-based pyramids connecting the centers of all 14 spheres forming a stacked lattice structure. A single pyramid, labeled ABCDE, is shown for reference.



Figure 5 CCPES model with pyramid lattice structure. Five pyramids form a stacked lattice structure connecting the centers of all 14 spheres. Total height (H_{RMS}) equals the stacked height of 2 pyramids plus the diameter (2r) of a single sphere.

Given that each side of the pyramid ABCDE = 2r, it can be shown that:

 $h = r\sqrt{2}$

Since:

$$H_{RMS} = 2r + 2h$$
$$= 2r\left(1 + \sqrt{2}\right)$$

Then the radius of a single sphere is:

$$r = \frac{H_{RMS}}{2\left(1 + \sqrt{2}\right)}$$

And the area of the square flat base is:

$$A_{flat} = (6r)^2$$

 H_{RMS} can be approximated by [1]:

Equation 6

$$H_{RMS} \approx \frac{R_z}{2\sqrt{3}}$$

Where: R_z is the 10-point mean roughness in meters. If the data sheet reports average roughness, then R_a is used instead.

Practical Example

To test the accuracy of the model, board parameters from [5] was used. Measured data was obtained courtesy of [9]. The extracted de-embedded generalized modal S-parameter (GMS) data was computed from 2 inch and 8 inch single-ended stripline traces. They were originally measured from the CMP-28 40 GHz High-Speed Channel Modeling Platform [15].

The CMP-28 Channel Modeling Platform, shown in Figure 6, is an excellent platform for model development and analysis. It contains a total of 27 microstrip and stripline interconnect structures. All are equipped with 2.92mm connectors to facilitate accurate measurements with a vector network analyzer (VNA).



Figure 6 CMP-28 Modeling Platform from Wild River Technology. Photo credit Wild River Technology

The PCB was fabricated with Isola FR408HR material and reverse treated (RT) 1oz. foil. The dielectric constant (Dk) and dissipation factor (Df), at 10GHz for FR408HR 3313

material, was obtained from Isola's isoStack® web-based online design tool [10]. An example is shown in Figure 7.

Typical traces usually have a trapezoidal cross-section after etching due to etch factor. Since the tool does not handle trapezoidal cross-sections in the impedance calculation, an equivalent rectangular trace width was determined based on a 2:1 etch-factor (60 deg taper).

icoStock		Design name: CMP28	Total number of cores: -1					Nu	Number of signal layers: 1				Length	Frequency
Date: Sat Mar 28 2015 12:08:48			Total pressed thickness: 39.900				Nu	Number of reference planes: 3				mils	10GHz	
	Thickness		Ref. plane	Zo	Diff Z	Tpd	Width	Spacing) Fill	Weight	Dk	Df	Build	Туре
1	1.400		true	na	na	na	5.000	10.000	100	1				
	10.600										3.59	0.0095	3x3313-57.0	FR408HR
2	1.250		false	49.0	98.0	161	10.380	10015.0	00 5	1				
	12.000										3.65	0.0094	3x3313	FR408HR
3	1.250		true	na	na	na	5.000	10.000	100	1				

Figure 7 Example of Isola's isoStack[®] online software used to determine dielectric thicknesses, *Dk*, *Df* and characteristic impedance for the CMP-28 board.

The default foil used on FR408HR core laminates is MLS, Grade 3, controlled elongation RTF. Roughness R_z parameters for drum and matte sides are 120µin (3.048 µm) and 225µin (5.715µm) respectively for 1 oz. copper [11].

An oxide or micro-etch treatment is usually applied to the copper surfaces prior to final lamination. This provides enhanced adhesion to the prepreg material. CO-BRA BOND® [12] or MultiBond MP [13] are two examples of oxide alternative micro-etch treatments commonly used in the industry today. Typically 50 μ in (1.27µm) of copper is removed when the treatment is completed, depending on the board shop's process control.

The etch treatment creates a surface full of micro-voids which follows the underlying rough profile and allows the resin to squish in and fill the voids providing a good anchor. Because some of the copper is typically removed during the micro-etch treatment, the published roughness parameter of the matte side is reduced by nominal 50 μ in (1.27 μ m) for a new thickness of 175 μ in (4.445 μ m).

Figure 8 shows SEM photos of typical surfaces for MLS RT foil courtesy of [11]. The left and center photos are the treated drum side and untreated matte side respectively. The right photo is a 5000x SEM photo of the matte side after etch treatment showing microvoids.



Figure 8 Example SEM photos of MLS RT foil courtesy of Oak-mitsui [11]. Left is the treated drum side and center is untreated matte side. SEM photo on the right is the matte side after etch treatment.

The data sheet and design parameters are summarized in Table 1. Respective *Dk*, *Df*, core, prepreg and trace thickness were obtained from the isoStack® software, shown in Figure 7. R_z of the matte side after micro-etch treatment ($R_z = 4.443 \mu m$) was used to determine K_{SR_matte} .

Parameter	FR408HR/RTF				
Dk Core/Prepreg	3.65/3.59 @10GHz				
Df Core/Prepreg	0.0094/0.0095 @ 10GHz				
R_z Drum side	3.048 μm				
R_z Matte side before Micro-etch	5.715 μm				
R_z Matte side after Micro-etch	4.445 μm				
Trace Thickness, t	31.730 μm				
Trace Etch Factor	2:1 (60 deg taper)				
Trace Width, w	11 mils (279.20 μm)				
Core thickness, H1	12 mils (304.60 μm)				

Table 1 CMP-28 test board parameters obtained from manufacturers'	data sheets and design
objective.	

Parameter	FR408HR/RTF					
Prepreg thickness, H2	10.6 mils (269.00 µm)					
GMS trace length	6 in (15.23 cm)					

Keysight EEsof EDA ADS software [14] was used for modeling and simulation analysis. The controlled impedance line (CIL) model allows modeling of trapezoidal traces.

Figure 9 is the general schematic used for analysis. There are three transmission line substrates; one for dielectric loss; one for conductor loss and the other for total loss without roughness.



Figure 9 Keysight EEsof EDA ADS generic schematic of controlled impedance line designer used in the modeling and simulation analysis.

Dielectric loss was modeled using the Svensson/Djordjevic wideband Debye model to ensure causality. By setting the conductivity parameter to a value much-much greater than the normal conductivity of copper ensures the conductor is lossless for the simulation. Similarly the conductor loss model sets the Df to zero to ensure lossless dielectric.

Total insertion loss (IL) of the PCB trace, as a function of frequency, is the sum of dielectric and rough conductor insertion losses.

Equation 7

$$IL_{rough}(f) = K_{SR_avg}(f)(IL_{smooth}(f)) + IL_{diel}(f)$$

To accurately model the effect of roughness, the respective roughness correction factor (K_{SR}) must be multiplicatively applied to the AC resistance of the drum and matte sides of the traces separately. Unfortunately ADS, and many other commercial simulators, do not allow access to these surfaces to apply the correction properly. The best you can do is to apply the average of (K_{SR}_drum) and (K_{SR}_matte) side to the smooth conductor loss (IL_{smooth}) , as described above.

The following are the steps to determine $K_{SR_avg}(f)$ and total IL with roughness:

1. Determine $H_{RMS_{drum}}$ and $H_{RMS_{matte}}$ from Equation 6.

$$H_{RMS_drum} \approx \frac{R_{z_drum}}{2\sqrt{3}}; \ H_{RMS_matte} \approx \frac{R_{z_matte}}{2\sqrt{3}}$$

2. Determine the radius of spheres for drum and matte sides:

$$r_{drum} = \frac{H_{RMS_drum}}{2\left(1+\sqrt{2}\right)}; \quad r_{matte} = \frac{H_{RMS_matte}}{2\left(1+\sqrt{2}\right)}$$

3. Determine the area of the square flat base for drum and matte sides:

$$A_{flat_drum} = (6r_{drum})^2; \quad A_{flat_matte} = (6r_{matte})^2$$

4. Determine $K_{SR_drum}(f)$ and $K_{SR_matte}(f)$:

$$K_{SR_drum}(f) = 1 + 84 \left(\frac{\left(\frac{\left(\pi r_{drum}^{2}\right)}{A_{flat_drum}}\right)}{\left(1 + \frac{\delta(f)}{r_{drum}} + \frac{\delta^{2}(f)}{2r_{drum}^{2}}\right)} \right)$$
$$K_{SR_matte}(f) = 1 + 84 \left(\frac{\left(\frac{\left(\pi r_{matte}^{2}\right)}{A_{flat_matte}}\right)}{\left(1 + \frac{\delta(f)}{r_{matte}} + \frac{\delta^{2}(f)}{2r_{matte}^{2}}\right)} \right)$$

5. Determine the average $K_{SR_drum}(f)$ and $K_{SR_matte}(f)$:

$$K_{SR_avg}(f) = \frac{K_{SR_drum}(f) + K_{SR_matte}(f)}{2}$$

6. Apply Equation 7 to determine total insertion loss of the PCB trace.

$$IL_{rough}(f) = K_{SR_avg}(f)(IL_{smooth}(f)) + IL_{diel}(f)$$

Summary and Results

The results are plotted in Figure 10. The left plot compares the simulated vs measured insertion loss for data sheet values and design parameters. Also plotted is the total smooth insertion loss (crosses) which is the sum of conductor loss (circles) and dielectric loss (squares). Remarkably there is excellent agreement up to about 30GHz by just using algebraic equations and published data sheet values for *Dk*, *Df* and roughness.

The plot shown on the right is the simulated (blue) vs measured (red) effective dielectric constant (*Dkeff*). As can be seen, *Dkeff* measured is 3.76 @ 10GHz, which is approximately 3.6% higher, compared to *Dkeff* simulated of 3.63 @ 10GHz. This is consistent with observations of increased phase velocity proportional to roughness profile and material thickness when tested in circuit applications as reported in [17].

When the measured *Dkeff* (3.76) was used in the model, for core and prepreg, the IL results shown in Figure 11 (left) are even more accurate up to approximately 50 GHz!



Figure 10 IL (left) for a 6 inch trace in FR408HR RTF using supplier data sheet values for Dk, Df and R_z . Effective Dk measured (red), and simulated (blue) is shown right.



Figure 11 IL (left) for a 6 inch trace in FR408HR RTF and effective *Dk* measured (red), and simulated (blue) is shown right.

Figure 12 compares the CCPES model against the H&J model. The results show that the H&J is only accurate up to ~ 15 GHz compared to the CCPES model's accuracy to ~ 50GHz.



Figure 12 CCPES Model (left) vs Hammerstad-Jensen model (right).

Conclusions:

Using the concept of cubic close-packing of equal spheres to model copper roughness, a practical method to accurately determine sphere size and tile area was devised for use in the Huray model. By using published roughness parameters and dielectric properties from manufacturers' data sheets, it has been demonstrated that the need for further SEM

analysis or experimental curve fitting, may no longer be required for preliminary design and analysis.

When measurements from CMP-28 modeling platform, fabricated with FR408HR and RT foil, was compared to this method, there was excellent correlation up to approximately 50GHz, compared to the H&J model accuracy to 15GHz.

The CCPES model looks promising for a practical alternative to building a test board and extracting fitting parameters from measured results to predict insertion loss due to surface roughness.

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References

- [1] Simonovich, B., "Practical Method for Modeling Conductor Surface Roughness Using Close Packing of Equal Spheres", DesignCon 2015 Proceedings, Santa Clara, CA, 2015, URL: <u>http://lamsimenterprises.com/Copyright2.html</u>
- [2] Hammerstad, E.; Jensen, O., "Accurate Models for Microstrip Computer-Aided Design," *Microwave symposium Digest, 1980 IEEE MTT-S International*, vol., no., pp.407,409, 28-30 May 1980 doi: 10.1109/MWSYM.1980.1124303
 URL: <u>http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1124303&isnum ber=24840</u>
- [3] S. Hall, H. Heck, "Advanced Signal Integrity for High-Speed Digital Design", John Wiley & Sons, Inc., Hoboken, NJ, USA., 2009
- [4] Huray, P. G. (2009) "The Foundations of Signal Integrity", John Wiley & Sons, Inc., Hoboken, NJ, USA., 2009
- [5] Shlepnev, Y., "PCB and package design up to 50 GHz: Identifying dielectric and conductor roughness models", The PCB Design Magazine, February 2014, p. 12-28. URL: <u>http://iconnect007.uberflip.com/i/258943-pcbd-feb2014/12</u>
- [6] Shlepnev, Y., "Sink or swim at 28 Gbps", The PCB Design Magazine, October 2014, p. 12-23. URL: <u>http://www.magazines007.com/pdf/PCBD-Oct2014.pdf</u>

- [7] Bogatin, E., DeGroot D., Huray, P. G., Shlepnev, Y., "Which one is better? Comparing Options to Describe Frequency Dependent Losses", DesignCon2013 Proceedings, Santa Clara, CA, 2013.
- [8] Wikipedia, "Close-packing of equal spheres". URL: http://en.wikipedia.org/wiki/Close-packing_of_equal_spheres
- [9] Simberian Inc., 3030 S Torrey Pines Dr. Las Vegas, NV 89146, USA. URL: http://www.simberian.com/
- [10] Isola Group S.a.r.l., 3100 West Ray Road, Suite 301, Chandler, AZ 85226. URL: <u>http://www.isola-group.com/</u>
- [11] Oak-mitsui 80 First St, Hoosick Falls, NY, 12090. URL: http://www.oakmitsui.com/pages/company/company.asp
- [12] Electrochemicals Inc. CO-BRA BOND®. URL: <u>http://www.electrochemicals.com/ecframe.html</u>
- [13] Macdermid Inc., Multibond. URL: <u>http://electronics.macdermid.com/cms/products-services/printed-circuit-board/surface-treatments/innerlayer-bonding/index.shtml</u>
- [14] Keysight Advanced Design System (ADS) [computer software], (Version 2016). URL: <u>http://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=US&lc=eng</u>
- [15] Wild River Technology LLC 8311 SW Charlotte Drive Beaverton, OR 97007. URL: <u>http://wildrivertech.com/home/</u>
- [16] Simonovich, B., "Practical Method for Modeling Conductor Surface Roughness Using The Cannonball Stack Principle", White Paper, Issue 1.0, April 8, 2015, URL: <u>http://lamsimenterprises.com/Copyright.html</u>
- [17] Horn III, A. F., LaFrance, P. A., Caisse, C. J., Coonrod, J. P., Fitts, B. B., "Effect of Conductor Profile Structure on Propagation in Transmission Lines", DesignCon2016 Proceedings, Santa Clara, CA, 2016